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# Dynamic Power Consumption In CMOS N Bit Full-Adder Circuit

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K E Y W O R D S

CMOS, Dynamic power, Full adder.

A B S T R A C T

*This paper discusses power consumption in the full adder circuit using some fabrication technologies. Though many studies related to power consumption in the full adder circuit were performed, however, few investigations about the effect of the number of bits on the power consumption are addressed. In this paper, the effect of changing the number of bits on the power consumption and time delay of the full adder circuit will be observed and the effect of changing the technology size is going to be calculated. The results will show that there is a direct relationship between the number of bits and power.*

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## 1. INTRODUCTION

The energy efficiency feature is an essential part of new electronic systems designed for high-performance or portable applications that users currently consider to be the main part of any design. On the other hand, the market segment constantly requires portable electronic devices that provide lower-power constructing blocks that allow the execution of long-permanent battery-powered systems as well as operating quickly [1]. The increased demand for low-power devices is using chip designers to cut down on devices with higher computational performance and longer battery life. The dissipated power in CMOS comes mainly from the dynamic power which is described by [2]:

$$p_d = F.C_L.\alpha.VDD^2 \quad (1)$$

Where F is the switching frequency. $C_L$ is the carrying capacity, $\alpha$ is the activity factor (describes the time duration in which the circuit changes its state within the frequency period [3]), VDD is the

supply voltage. The lower the voltage, the lower the power consumption. Transistors PMOS and NMOS are the logic circuits of CMOS. Full adder is an essential component in the logic circuit [4].

Most full adder systems use XOR, NAND, and XNOR logic gates. The literature [5]–[9] provided performance driving capability for various low-power full adders.

As far as we know this paper is the first to study the effect of technology and the number of bits on the energy model. This paper will be organized as follows: in section one we will explain the power dissipation in conventional CMOS circuits, and in section two we will explain the review of the dynamic power model. In the third section, we will explain the simulation results in a standard CMOS process technology, and we will also make a comparison between our results and the results of other researcher's works then we will explain how we calculated the power of the 1-bit full adder circuit, and then the multi-bit full Adder, and also the effect of time delay on the full adder circuit, finally we will make some conclusions in the final section.

## 2. POWER DISSIPATION IN CMOS CIRCUIT

The full Adder consists of 3 inputs and 2 outputs. Three bits be added at one time. The A and B bits to be added from both input and the third input of the load created by the previous addition. Resulting in outputs: sum and carry. The simplified term for the sum of the output variables (sum) and the load output (Cout) is expressed in the following equations [5]. Figure1 represents the structure of full adder circuit and Figure2 represented structure of full adder in CMOS circuit. Semiconductor industry is ready to downscale Complementary Metal Oxide Semiconductor (CMOS) transistors which has formed denser, cheaper, faster, smaller, and functionality richer electronic devices[10].

$$sum = (A \oplus B) \oplus C_{in} \quad \text{(2-a)}$$

$$C_{out} = A.B + C_{in}.(A \oplus B) \quad \text{(2-b)}$$

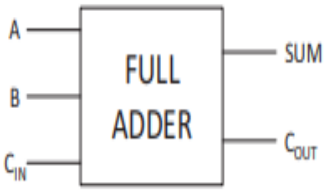


**Figure 1: Full adder structure**

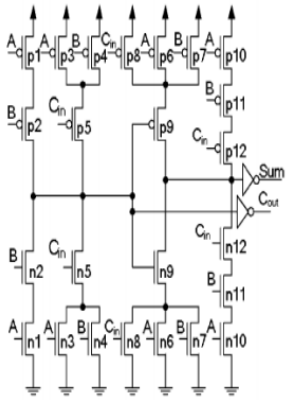


**Figure 2: CMOS Full Adder**[11]

The type that we relied on and used in our results is dynamic power, which we will explain in detail in the next section**.**

### *I. Dynamic power*

Dynamic power is the energy required to charge and discharge the capacitance load on the transistor gates in the circuit. When the circuit is in operation, it means that the consumed energy is dynamic, that is, the circuit performs some task on some data. Dynamic power dissipation is caused by switching signals from low to high and high to low in circuits[12][13]. The dynamic power is given by equation (1).

## 3. REVIEW OF DYNAMIC POWER MODEL

Equation (1) describes the dynamic behavior of one logic gate, which is not the case when looking at a whole digital circuit. The effect of each gate on the system must be calculated so that it is possible to predict the power consumed in the circuit. To include the effect of all the logic gates in the circuit, equation (1) should be reformated into [13]–[15]

$$P_d = \alpha . C_L . V_{dd}^2 . F \sum_{i=1}^{n} C_{Li} \quad (٣)$$

Where i in equation (٣) is considered some gates and $C_{Li}$ is the load capacitance for each gate.

Another important part to consider when talking about power consumption in a digital CMOS circuit is the time delay. Each gate in the logic circuit is connected to multiple gates, and each gate has a unique time delay called (td) that depends on the number of inputs and outputs. Sometimes researchers call it the time taken to go from inputs to output. and can be expressed by [16].

$$t_d = \frac{C_L V_{DD}}{\mu . C_{OX} . \frac{W}{L} . (V_{DD} - V_{th})^2} \quad (٤)$$

Where μ is carrier mobility, $C_{OX}$ is the oxide capacitance, $\frac{W}{L}$ is the width to length ratio of the transistor and $V_{th}$is the threshold voltage. It is shown from (٤) that as $V_{DD}$ decreases, td increases. This means that the relationship between the time delay and the voltage is an Inverse relationship.

It should be noted that if the reciprocal of the frequency of the system (clock) is less than that of the time delay of the gate, the transition between 0 to 1 will not occur and hence no power is dissipated in the operation (it also means that the output is errorless)[1]

one of the key parameters that influence dynamic power is the load capacitor($C_L$)which, if reduced, minimizes not only the power but also the time delay of the logical gates in the circuit, as shown in equation(٥).

$$C_L = C_{DP} + C_{Dn} \quad (٥)$$

This equation can be seen in[17] Where $C_{DP}$is the capacitor for p substrate drain, and $C_{Dn}$is the capacitor for n substrate. The equation above (٥) is only true if the port is not linked to another gate or load. And this equation (٥) is modified to accept output stage input capacitance and will become as

$$C_L = C_{DP} + C_{Dn} + C_{GP} + C_{Gn} \quad (٦)$$

$C_{GP}$and $C_{Gn}$ are the capacitance of the p and n gate substrates.

Looking closely at the equation (٦) and taking into account the probability of linking the logic gate to more than one gate at a time, one can deduce the following formula [15]

$$C_L = C_{DP} + C_{Dn} + no.(C_{GP} + C_{Gn}) \quad (٧)$$

Where (no) is the fan-out (number of connected exit gates).

$C_{Gn}$and $C_{Gp}$ could be determined from the [1]

$$C_{Gi} = W_i . l_i . C_{ox} \quad (٨)$$

While the $C_{Dn}$and $C_{DP}$are given

$$C_{Di} = C_{Dio} . W_i \quad (٩)$$

Where i is either n or p and $W_i$, $l_i$is the width and length of the IMOS transistor. $C_{Dio}$ is a constant according to the equipment used. Where $C_{ox}$is the oxide capacitance and the $T_{ox}$ is the thickness of the oxide can be estimated from [15].

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \quad (١٠)$$

$\varepsilon_{ox}$ is given by:

$$\varepsilon_{ox} = 3.9.\varepsilon_0 \quad (1١)$$

$\varepsilon_0$ is the permittivity of the free space and is equal to 8.854x10-12 (F/M2).

Table I represented parameters used in simulation

**Table I: the parameters used corresponding to the technologies** [18]–[21]

| Technology | $T_{ox}$ | $V_{tn}$ | $V_{tp}$ | $u_{en}$ | $u_{ep}$ |
|---|---|---|---|---|---|
| *180nm* | 4e-9 | 0.399 | -0.42 | 35e-3 | 8e-3 |
| *90nm* | 2.05e-9 | 0.397 | -0.339 | 0.0547 | 0.00711 |
| *45 nm* | 1.8e-009 | 0.62261 | -0.587 | 0.049 | 0.021 |
| *32 nm* | 1.6e-009 | 1.6e-009 | -0.5808 | 0.042 | 0.016 |
| *22 nm* | 1.4e-009 | 0.68858 | -0.63745 | 0.035 | 0.011 |
| *16 nm* | 1.2e-009 | 0.68191 | -0.6862 | 0.028 | 0.0075 |

## 4. THE BASIC MODULE OF FULL ADDER

The attached table, herewith, explains the main components of the full adder. Multiple full adder circuits consist of cascaded full adders to add N-bit numbers; there are N full adder circuits cascaded in parallel. Any adder gives two outputs one is called sum and the other is called carry, this output carry is defined as carry out[22] .

**Table II: Truth table of full adder**

| A | B | $C_{in}$ | Sum | $C_{out}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

The entire architecture of the CMOS adder is implemented with transistor PMOS and NMOS stacks. Usually, optical arithmetic circuits such as adders are built with NAND or NOR gates instead of AND, OR gates. NAND and NOR gates are used in all integrated circuit families and are simpler to fabricate with electronic components. It is therefore easy to convert NO, AND, and OR gates into an equivalent NAND and NOR logic diagram[23].Figure 3 represented full adder circuit with NAND gates

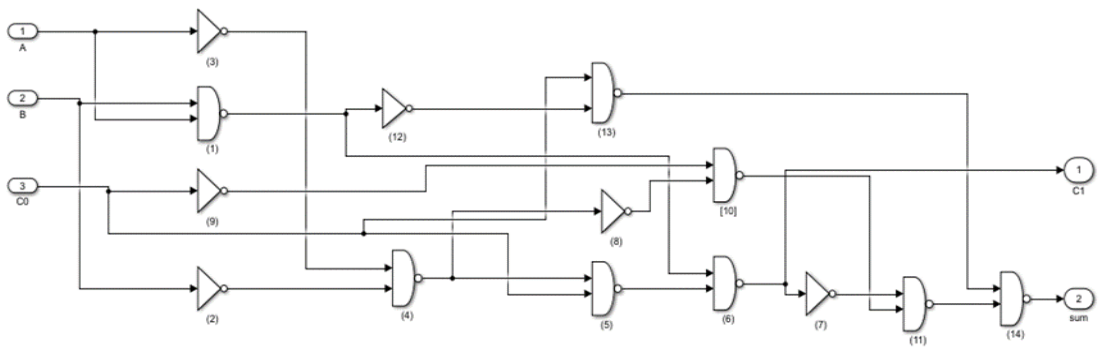


**Figure 3: Gate Level Implementation of the full adder**

For the given circuit, the signal propagation paths for any gate are represented in Table III and Table IV.

**Table III: For the Sum Output**

| Path number | Gates | Connected to $C_{n-1}$ |
|---|---|---|
| | (13),(14) | Yes |
| | (1),(12),(13),(14) | No |
| | (1),(6),(7),(11),(14) | No |
| | (3),(4),(5),(6),(7),(11),( 14) | No |
| | (2),(4),(5),(6),(7),(11),(14) | No |
| | (5),(6),(7),(11),(14) | Yes |
| | (9),(10),(11),(14) | Yes |
| | (3),(4),(8),(10),(11),(14) | No |
| | (2),(4),(8),(10),(11),(14) | No |

**Table IV: For the C1 output**

| Path number | Gates | Connected to $C_{n-1}$ |
|---|---|---|
| | (1),(6) | No |
| | (3),(4),(5),(6) | No |
| | (2),(3),(4),(5),(6) | No |
| 1. | (5),(6) | Yes |

The paths that are a marker in red are the paths that are linked to the sum of the previous full adder stage. Table V represented fan out of each gate for the full adder circuit.

**Table V: The Fan out of each gate**

| Gate | Fan out |
|---|---|
| (1) | 2 |
| (2) | 1 |
| (3) | 1 |
| (4) | 2 |
| (5) | 1 |
| (6) | 2 |
| (7) | 1 |
| (8) | 1 |
| (9) | 1 |
| (10) | 1 |
| (11) | 1 |
| (12) | 1 |
| (13) | 1 |

Fan out is consider number of connected exit gates for any gate, $C_L$ is computed using the equations (7) we explained in the previous section.

## 5. SIMULATION RESULT AND THE COMPARISON WITH OTHER PAPERS

Using equation (1) (٤) (٧) we build an algorithm and this equation is succeeded in determining the relationship between voltage, frequency, gate time delay, transistor size, and dynamic power connections. MATLAB is used to perform this algorithm to measure circuit power and time delay. The circuit used Shown in figure 3

The simulation was performed using several techniques (45, 22, and 16,180) nm while the voltages used are (0.9, 1.2, 1.5, 2, and 2.5) V First, we apply circuit figure (3) to the 16 nm technique. Figure (4) will illustrate the dynamic power consumption. Figure (5) will indicate the average time delay for the full adder circuit used for the different voltages of the new model using MATLAB.

Figure 6 shows the power dissipation of a 22 nm one-bit FA circuit. The time delay is illustrated in figure (7). And figure (8) shows the power dissipation of a 45 nm one-bit FA circuit. The time delay is illustrated in figure (9). In the final figures (10) (11) the result of one bit FA for 180 nm. From the previous figures, we notice that the energy becomes low as the size of the technology decreases. Any less power consumption is when using 16 nm technology, and the power consumption begins to increase as the size of the technology increases. That is, the relationship between the size of technology and power is a direct one. The lower the technology, the lower the power. At the same time, the lower the value of the technology, the less the time delay is. Therefore, we always prefer to use the value of the technology less.

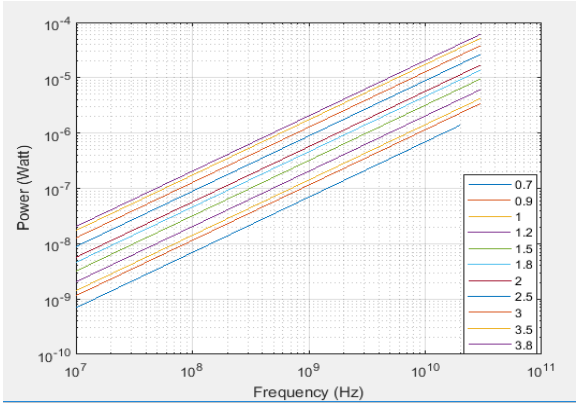


**Figure 4: Dynamic power Dissipation Vs Frequency of 16nm 1-Bit FA Using the MATLAB**

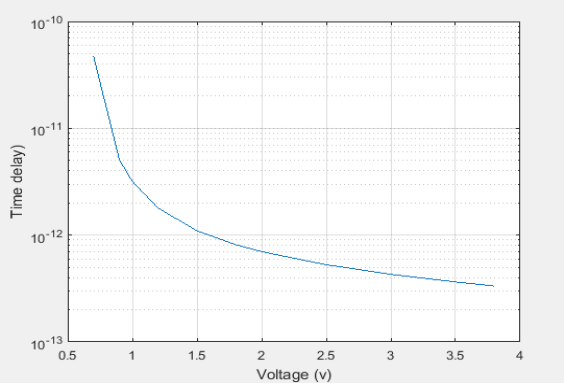


**Figure 5: Time Delay of 16nm 1-Bit FA Using the Power Model**

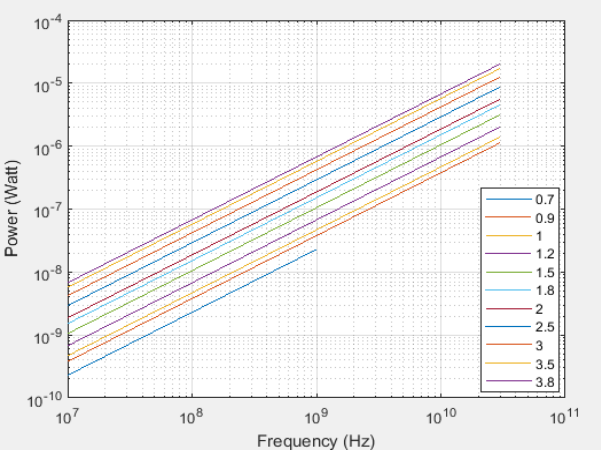


**Figure 6: Dynamic power Dissipation Vs Frequency of 22nm 1-Bit FA Using the MATLAB**

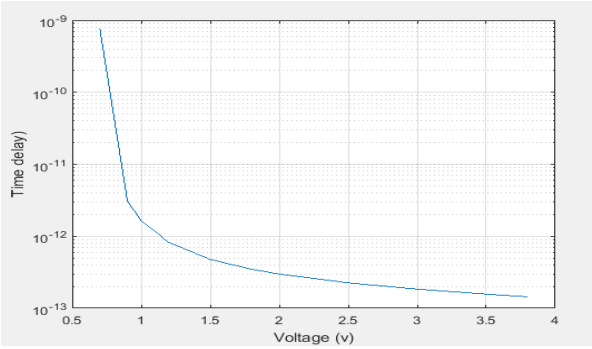


**Figure 7: Time Delay of 22nm 1-Bit FA Using the Power Model**

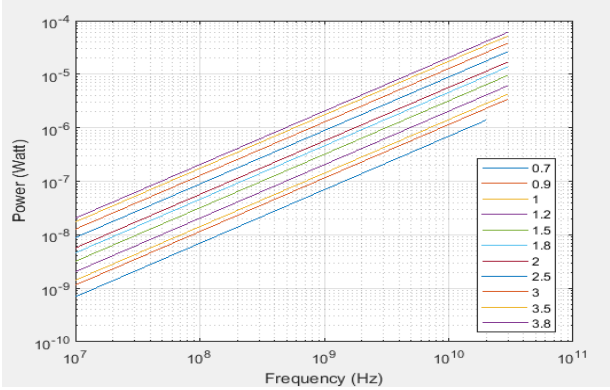


**Figure 8: Dynamic power Dissipation Vs Frequency of 45nm 1-Bit FA Using the MATLAB**

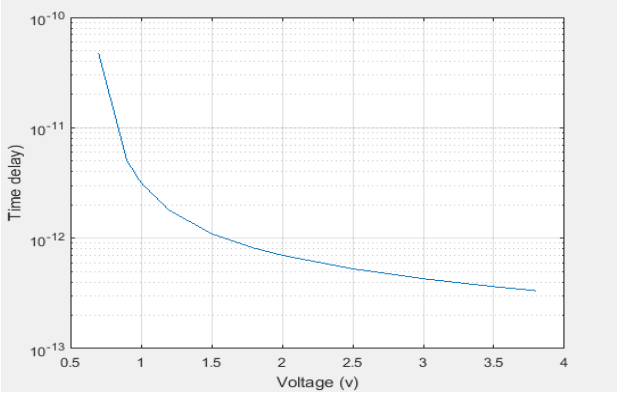


**Figure 9: Time Delay of 45nm 1-Bit FA Using the Power Model**

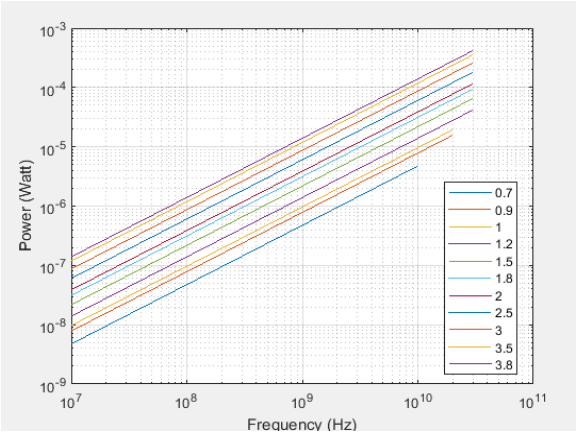


**Figure 10: Dynamic power Dissipation Vs Frequency of 180nm 1-Bit FA Using the MATLAB**

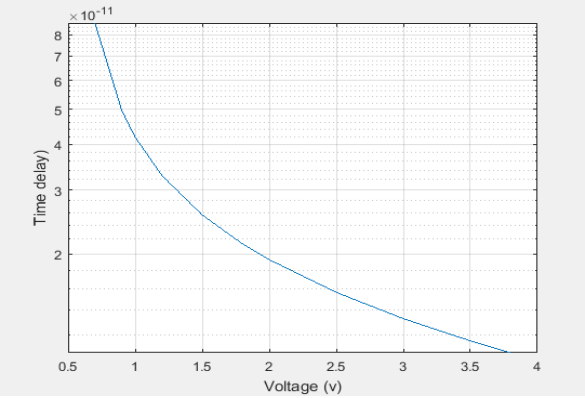


**Figure 11: Time Delay of 180nm 1-Bit FA Using the Power Model**

In figure (12), the amount of the three technologies 16, 22, and 45 were compared, and it becomes clear that the greater the amount of voltage (0.9, 1.2, 1.5, 2, 2.5) the greater the amount of power because the relationship between voltage and energy is positive according to equation (1). At the same time, the lower the value of the technology (16, 22, 45) the less the power.

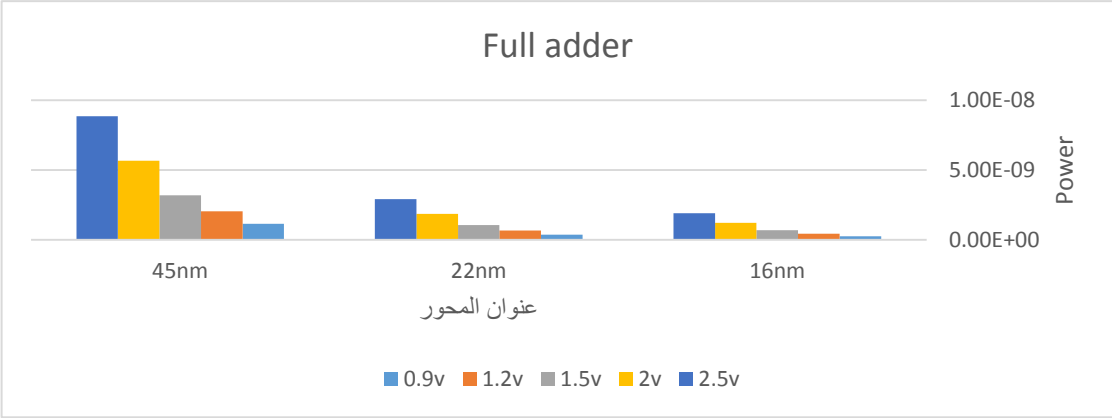


**Figure 12: Dynamic power Dissipation Vs Frequency 1-Bit FA Using the MATLAB**

Likewise, in figure (13) the values of the technologies (16, 22, and 45) are compared to illustrate what happens to the time delay, in one bit. In flip-flop, it is found that as the voltage value increases, the time delay decreases, which means that the inverse relationship between time delay and voltage is according to equation (4). Likewise, the lower the value of the technology, the lower the time delay value.

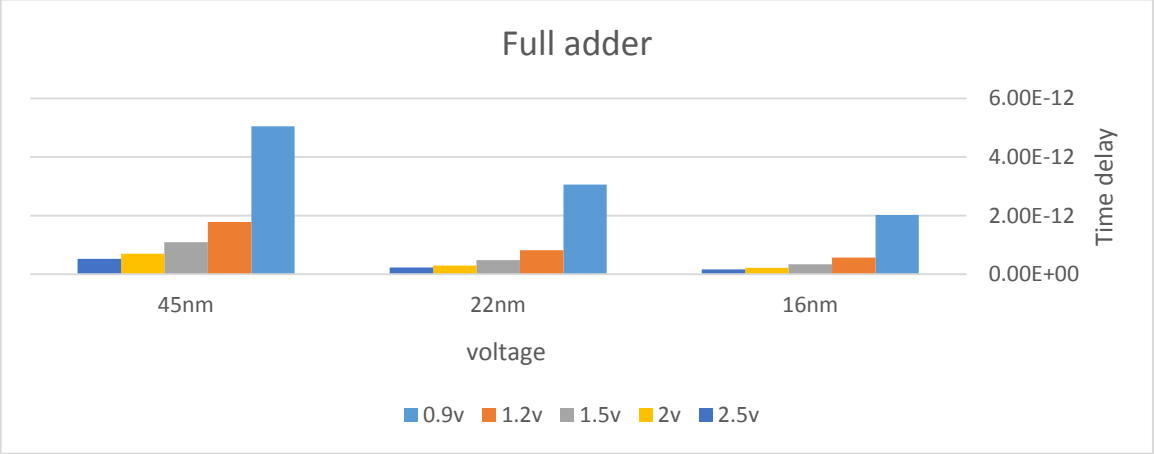


**Figure 13: Time Delay 1-Bit FA Using the Power Model**

In the next section, we will explain what happens to power and time delay when the number of bits increases in full adder circuits.

In figures (14) and (15), the number of bits was increased to four, and several voltages were compared with different values (0.9, 1.2, 1.5, 2.5, and 2.5). Several techniques were selected and compared (45, 22, and 16). It was found that with the increase in the number of bits, the values of power and time delay increased, meaning that there is a direct relationship between the number of bits and the power, at the same time the speed increased significantly.

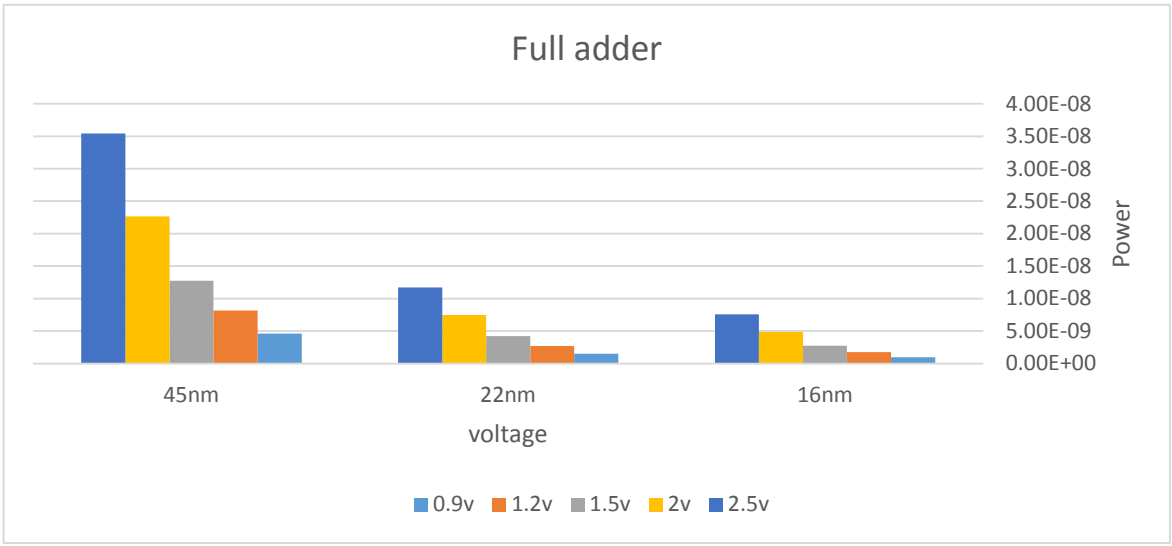


**Figure 14: Dynamic power Dissipation Vs Frequency 4-Bit FA Using the MATLAB**

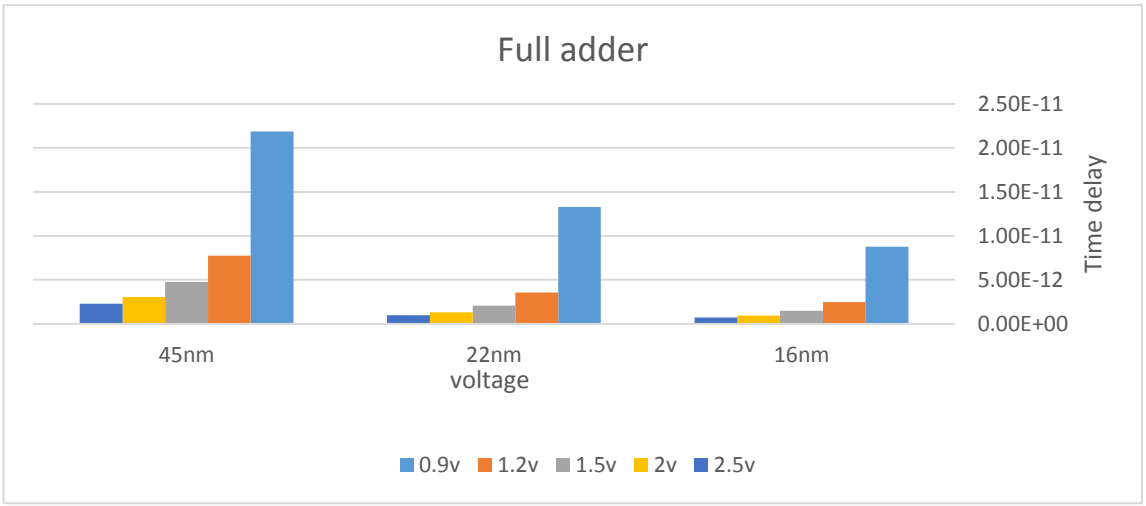


**Figure 15: Time Delay of 4-Bit FA Using the Power Model**

Likewise, we will observe what happens when the number of bits increases to 8 and 16 bit in the following figures. And it turns out that the more we start to increase the number of bits, the better the speed value will be, and this has been explained in figures (16) (17) (18) (19).

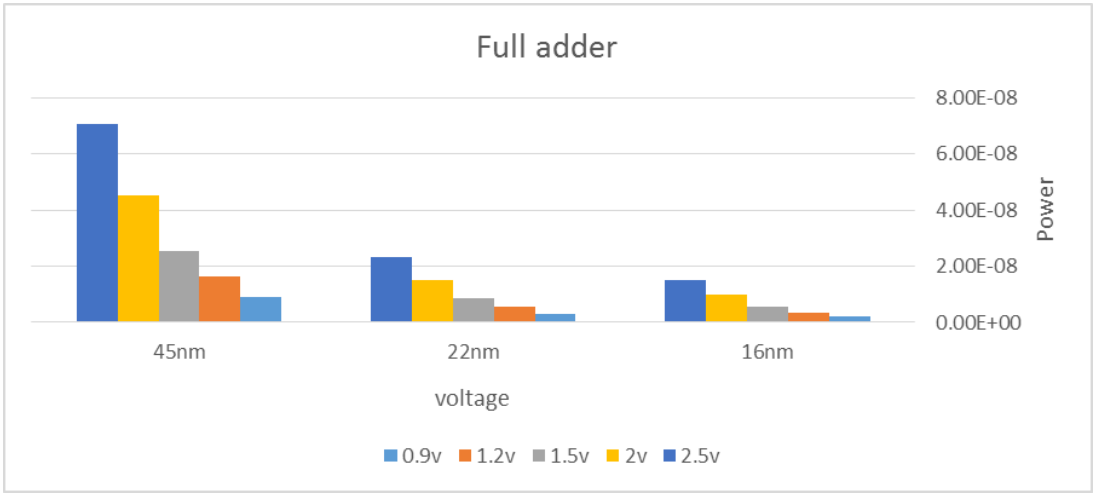


**Figure 16: Dynamic power Dissipation Vs Frequency 8-Bit FA Using the MATLAB**

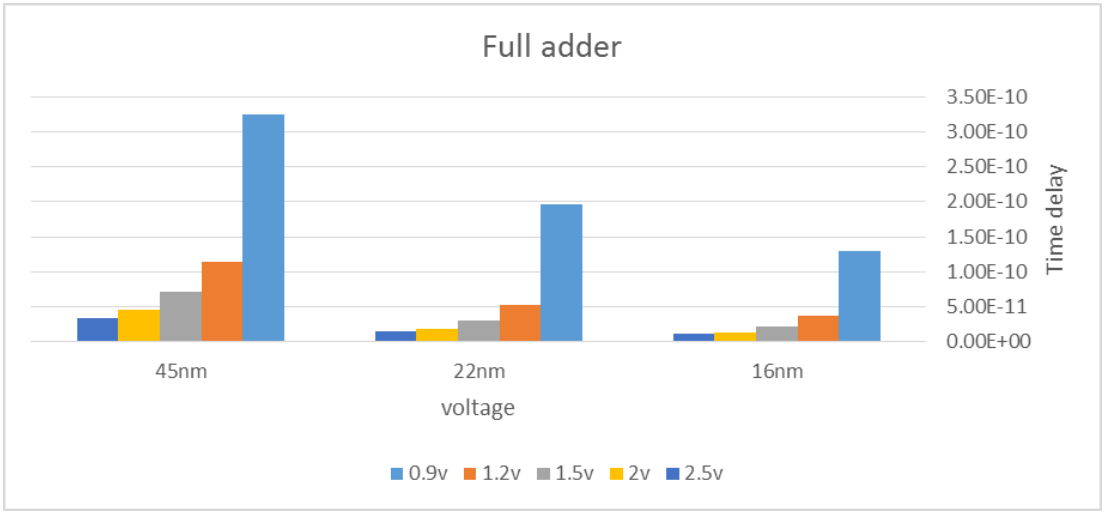


**Figure 17: Time Delay 8-Bit FA Using the Power Model**

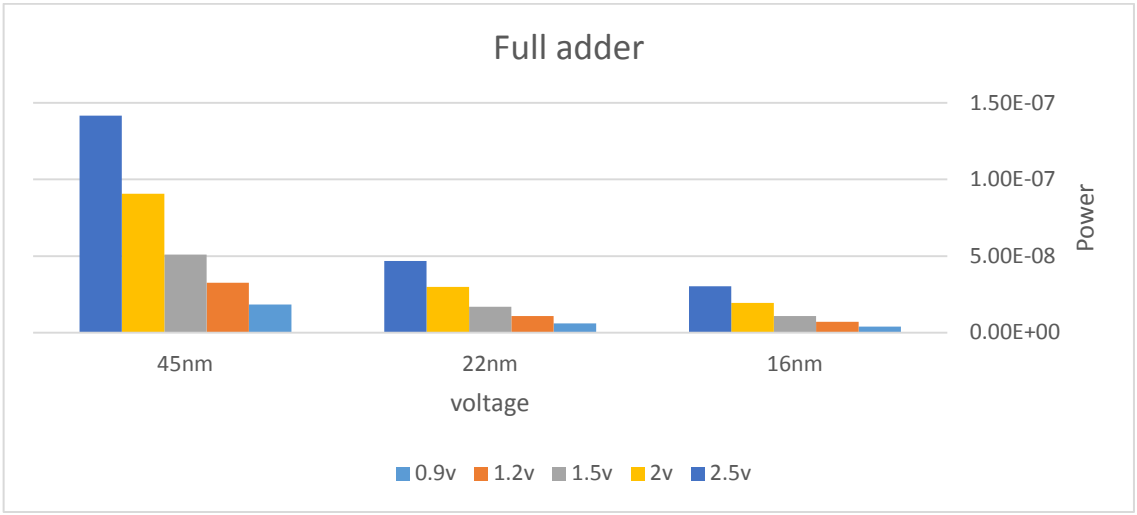


**Figure 18: Dynamic power Dissipation Vs Frequency 16- Bit FA Using the MATLAB**

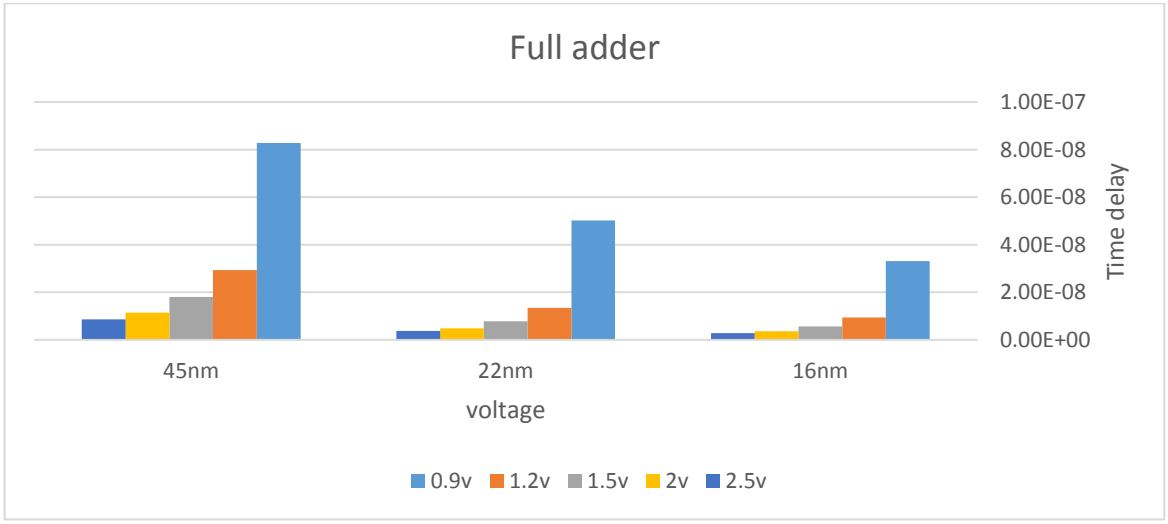


**Figure 19: Time Delay 16- Bit FA Using the Power Model**

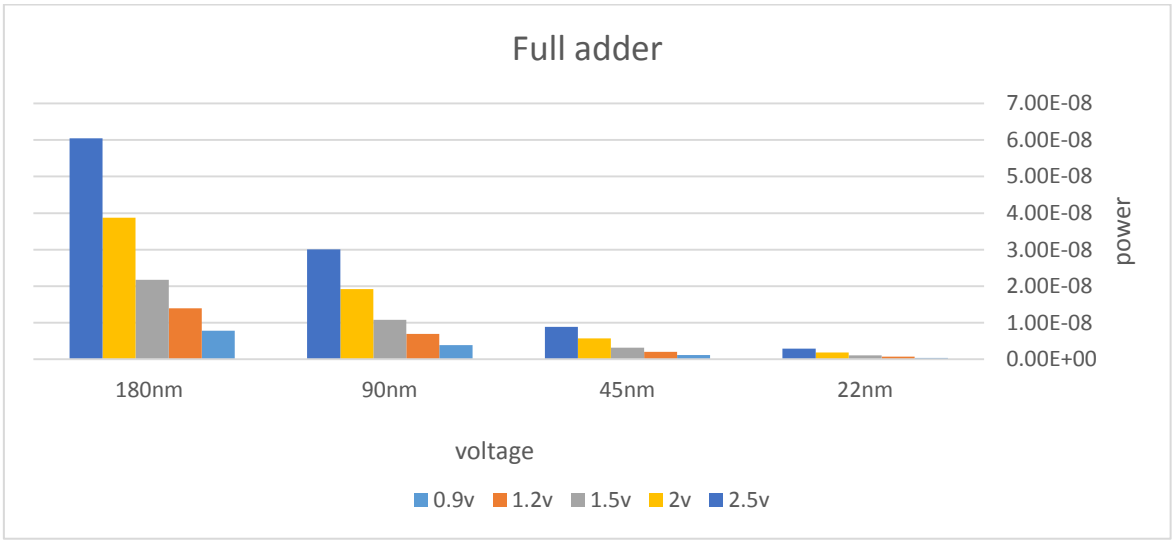


**Figure (20): Dynamic Power Dissipation Vs Frequency ١Bit FA Using the MATLAB 180nm, 90nm, 45nm, 22nm**

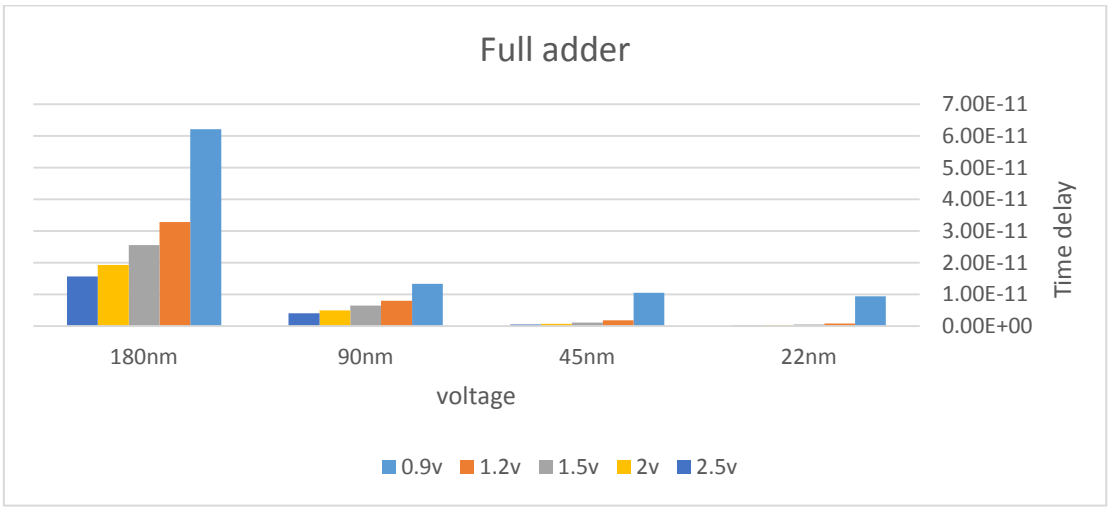


**Figure (21): Time Delay by Using the Power Model in one bit**

In the next section, we will explain the results of comparisons in Table VI, the first comparison was with the[24]. In this paper, the selected voltages were 1.5 and the resulting power value was close to or similar to the power value we obtained from our results. The frequency value was chosen 50 MHz

**Table VI: the comparison with 90nm Technology**

| Technology | Voltage | Frequency | Power from paper | Power |
|---|---|---|---|---|
| 90nm | 1.5V | 50 MHz | 54.72e-9 | 5.4059e-8 |

And the next paper used to comparison was [25] in Table VII. Voltage was chosen 1.8 and likewise, the frequency was 300 MHz the value of the technology used was 180nm. And the value of our results was close to the results of a paper.

**Table VII: the comparison with 180nm Technology**

| Voltage | Technology | Frequency | Power from paper | Power |
|---|---|---|---|---|
| 1.8 v | 180nm | 300 MHz | 6.2199e-6 | 6.5322e-6 |

In the last paper, it was a [9] in Table VIII, and our findings are shown in the next table.

**Table VIII: the comparison with 180nm Technology**

| Voltage | Technology | Frequency | Power from paper | Power |
|---|---|---|---|---|
| 0.8 v | 180nm | 100 MHz | 0.6126e-6 | 6.1935e-8 |

## 6. CONCLUSION

In this paper, we discussed the effect of the number of bits on energy consumption. Likewise in this paper, we observed the effect of changing the number of bits on energy consumption and time delay of the full adder circuit, and the effect of changing the technology size on both power and time delay, and the results showed that there is a direct relationship between the number of bits and the power.

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