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Improved Design for the High Gain Wideband Matrix Amplifiers Using Differential Cells and Microwave CMOS Technology

Saeed R. Saeed[a]*, Azad R. Kareem[b], Ashwaq Q. Hameed[a]

[a] Electrical Engineering Dept., University of Technology-Iraq, Alsina'a street, 10066 Baghdad, Iraq.
[b] Control and Systems Engineering Dept., University of Technology-Iraq, Alsina'a street, 10066 Baghdad, Iraq.
*Corresponding author Email: eee.18.15@grad.uotechnology.edu.iq

HIGHLIGHTS

- The Matrix Amplifier is a structure designed to increase the gain of the wideband distributed amplifiers.
- A promising method for the deployment of high-speed optical systems with completely integrated transceivers by utilizing CMOS-distributed amplifiers with bandwidths of gigahertz to a few tens of gigahertz
- The stable gain and excellent terminal match across a wide frequency range are the key reasons for the increased usage of distributed amplifiers.
- The solution to the gain bandwidth roll-off problem is in this paper.
- Decreasing the roll-off problem in which the values of the gain and BW are approximately balanced (High gain and high bandwidth).

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ABSTRACT

The Matrix Amplifier is a structure designed to increase the gain of the wideband distributed amplifiers. A matrix amplifier is used to improve the pass-band gain while preserving the dispersed design-wide characteristics to use the multiplicative gain mechanism. In this paper, the matrix distributed amplifier methodology is developed using differential cells instead of active amplifier cells to improve the wideband characteristics. Shunt capacitances are connected in the centerline to absorb the peaking impact at a cut-off frequency and reduce gain ripples. As an application of the ideas and concepts of matrix amplifiers, a modified step-by-step design of rows 4 and column 2 matrix amplifier is undertaken using a Quasi Differential amplifier. A Matrix differential amplifier using a shifted-second-tier structure technique is then built and tested in 0.18 µm Complementary Metal Oxide Semiconductors technology. The advantages gained from the proposed design are high gain, high bandwidth, low noise, and no need for balun circuits. The design and simulation results were achieved using ADS. The significant results show a high gain of 40 dB and a 33 GHz bandwidth. The noise figure is also 3.583, with S11, S22, and S12 being -10 dB, -10dB, and -40dB, respectively; the output power at 1-dB gain compression point is evaluated (P1dB) of +6.4 dBm, and the total DC power dissipation is 266mW. The cadence tools produced the layout design and specifications, although the chip size was 1.1mm^2.

1. Introduction

One of the most common broadband amplifier topologies is distributed amplifier (DA), sometimes called a traveling-wave amplifier. Distributed amplifier (DA) was first suggested by Percival in 1936 and further refined by Ganton in 1948 [1]. By introducing capacity from active devices into the synthetic transmission lines, the distributed amplifier achieves flat pass-band gain, high phase linearity, and perfect impedance properties throughout a large frequency range [2]. Although transistor technology has been provided most significant driver of gain and also bandwidth with microwave signals and RF amplifiers, and the product of gain with bandwidth (GBW) is constant; however, the transistors are physical environment (designed) affect and limits in which the practical gain and bandwidth of amplifiers [3]. The design cost of a radio frequency (RF) device is based on integration, and performance is cheap and enhanced by the force of nanoscale scaling complementary-metal-oxide-semiconductor (CMOS) technology [4]. The high-rate broadband communication systems need to use wideband amplifiers as critical building blocks. One of the most common alternatives for broadband amplification applications appears to be the

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distributed amplifier [5]. The high gain-bandwidth product and outstanding linearity, like distributed amplifiers (DA), make them a great choice for highly wideband amplification applications [6]. The amplifier's bandwidth can be restricted when utilizing gate and drain circuits transmission lines in which the main difficulty is distributed based-amplifier theory [7]. High GBW could be attained using interest growth methods if the problem of bandwidth constraint were overcome [8]. Concentration in each stage of a distributed amplifier is undoubtedly the simplest approach that raises appeal. The first conceivable solution is to enhance transconductance [9]. CMOS distributed amplifiers have received a lot of interest due to recent breakthroughs in deep subemicron manufacturing technology, leading to lower costs and a better degree of integration [10]. A promising method of deployment based on high-speed optical systems with completely integrated transceivers. Utilize the CMOS-distributed amplifiers with bandwidths of giga-hertz to a few tens of giga-hertz [11]. Because the disadvantage of additive gain operation and the lack of High-Q on-chip passive components restricted CMOS distributed amplifiers [12]. The purpose of this paper is to suggest a design for a Matrix Quasi Differential QD amplifier. This will allow the amplifier to take advantage of the differential amplifier features such as high BW and low noise; in addition, it eliminates a balun circuit, and the proposed technique is a single-ended input/output. The structure of the distributed amplifier is useful in many applications of microwave range, such as in radar, wireless, optical, and mobile communication systems—however, it utilizes design microwave switches [13].

2. Review

Many academics presented almost effective solutions to common distributed amplifier problems. In 2006, researchers suggested a two-by-four matrix amplifier created in a two-row, four-column, and three-layer metal 0.18 m SOI CMOS process. [14]. This design provides a 12.5 GHz unity-gain bandwidth and a 15 dB average pass-band gain. The SOI CMOS process design derived a half section that matches the input and output ports within 50 Ω based on S_11, and S_22 observed values of surpassing 7 and 12 dB, respectively. This design also consumed total power of 233.4 mW from 2.4V and 1.8V when integrated into 2.0 × 2.9 mm^2. In 2010, authors proposed a distributed 2 x 3 matrix amplifier with active post distortion and an ideal gate bias linearization strategy to eliminate broadband distortion in a fully integrated CMOS technique. According to simulation data, the S_21 power gain peaks at 7.1dB before rolling off to gain bandwidth of 16 GHz, returning a loss of less than -10 dB and S_12 isolation of less than -45 dB. The simulation results revealed 9 dBm IIP3 improvement at -10 dBm output power, translating to 18 dB third-order intermodulation IM3 suppression [15]. In 2017, authors offered the matrix single-stage distributed amplifier as a new amplifier topology (M-SSDA). The amplifier may have a lower gain-per-device than traditional distributed and matrix amplifiers since it only employs multiplicative gain. A two-tiered common-emitter (CE) M-SSDA based on a full-foundry double hetero-junction bipolar transistor (DHBT) model demonstrated the practicality of the proposed design. Simulations predict a 20dB gain at 324GHz bandwidth [16]. In 2020, researchers also demonstrated a tapered matrix distributed amplifier with perfect integration for broadband applications. TSMC's 180 nm CMOS RF technology created the distributed amplifier. The suggested distributed amplifier uses a matrix architecture that simultaneously uses the two multiplicative gain and additive gain processes to improve gain. Reduced power consumption is also achieved by the use of tapered transmission lines. In addition, a superior RL network replaces the terminating resistor on the input transmission line to enhance the DA's noise curve. To increase bandwidth, the gain cells in the initial stage of the distributed amplifier are adjustable cascade amplifiers. According to simulation data, the suggested distributed amplifier with a 3-dB bandwidth at 19.5 GHz produces a flat power gain (S_21) of 12 +¯1 dB. The DA's S_11 and S_22 are less than -10 dB at the specified frequency range. The noise figure (NF) operational range ranges from 5 to 6.75 dB [17].

3. Distributed Amplifier and Matrix Amplifier

Distributed amplifiers (DA) are used additive amplification to achieve wide bandwidth [18]. A matrix amplifier (MA) consists of simply two or more differential amplifiers stacked in a multiplicative manner. To achieve a decent performance and improved amplifier design that utilizes a multiplicative amplification in a 2-D array, this design is distributed the gain by which elements are used [19]. The most popular type of traditional distributed amplifiers (DA) with artificial transmission lines (discrete inductors) is shown in Figure 1 [20]. The constant -k^{th} of the filter coefficient is commonly used in artificial transmission lines. The image impedance terminates the amplifier gate and drain lines [21]. As shown in Figure 2, the matrix amplifier is made by one or more stages. The latter stage of the input line is a stacked distributed amplifier overlapping with the former output line. [22]. The module is mixed by additive and multiplicative amplification that is proved by the properties of a cascaded distributed amplifier [23]. There are many of several advantages [24]: 1) it takes up less chip area and can be easily implemented on a monolithic IC, 2) it has better input and output matching, 3) it should result in a lower noise figure, and 4) the phase delay is cut in half.

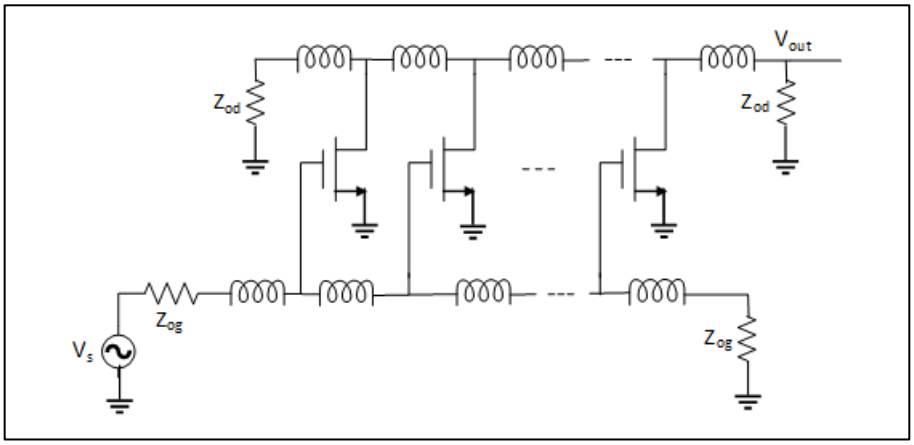


Figure 1: Conventional distributed amplifiers with artificial lines [20]

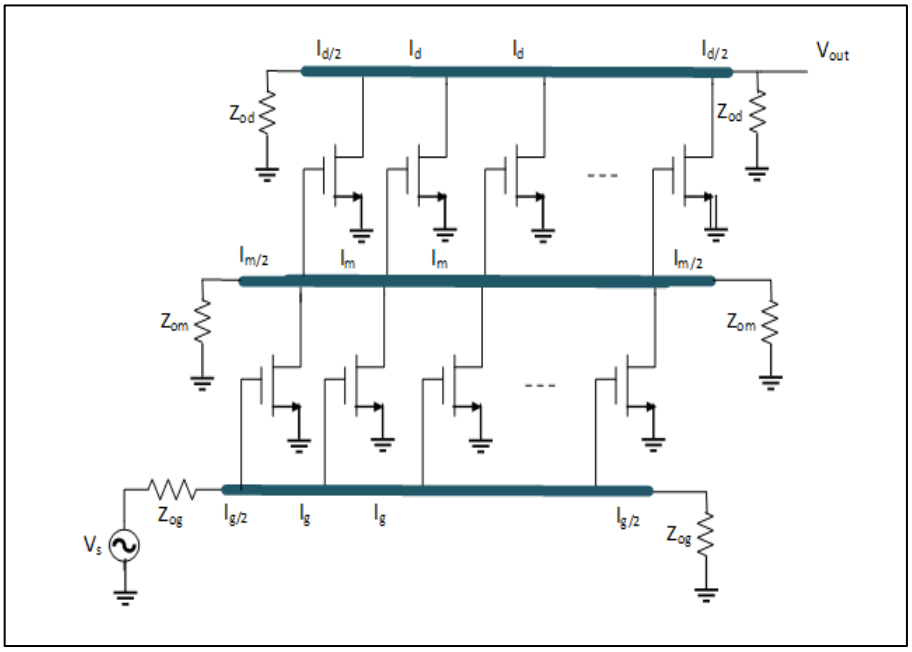


Figure 2: Example of matrix DA architecture consisting of two rows [22]

The stable gain and excellent terminal match across a wide frequency range are given decent reasons to increase the usage of DAs [23]. However, the worst scenario can be to misspend half of the output current from the FETs, allowing current to flow in the opposite direction down the drain line to the idle drain load end [24]. Moreover, the drain current might be sent into the output drain in real-world scenarios by simply tapering the resistance of the artificial transmission lines [25]. Furthermore, if the drain line is cut on the interior section of the final piece of equipment, the former current can flow in the reverse direction into the drain line in the best-case scenario. Obsolete, this technology can render all previous equipment; however, it can only produce a single-stage distributed amplifier. The amplifiers output current is provided by [26]:

$$I_{out} = \frac{1}{2} g_m e^{-\frac{\theta_d}{2}} \sum_{k=1}^{n} V_{ck}\, e^{-(n-k)\theta_d} \qquad (1)[24]$$

The voltage across the C_{gs} of the K[th] transistor is referred to V_{ck} The number of transistors is n, and the drain line propagation constant is $\theta_d = A_d + j\emptyset_d$. The V_{ck} whereas calculated by multiplying the voltage at the gate terminal of the kth FET by:

$$V_{ck} = \frac{V_i e^{-(2k-1)\theta_g/2 - j\tan^{-1}(\omega/\omega_g)}}{2\left[1+(\omega/\omega_g)^2\right]^{1/2}\left[1-(\omega/\omega_c)^2\right]^{1/2}} \qquad (2)[24]$$

Both lines' phase velocities must be same degree, as previously stated, to get a good gain as shown on outcome result as follow:

$$I_0 = \frac{g_m V_i \sinh\left[\frac{n}{2}\left(A_d - A_g\right)\right] e^{-n\left(A_d + A_g\right)/2 - jn\phi - j\tan^{-1}(\omega/\omega_g)}}{2\left[1+(\omega/\omega_g)^2\right]^{1/2}\left[1-(\omega/\omega_c)^2\right]\sinh\left[\frac{1}{2}\left(A_d - A_g\right)\right]} \quad (3)[24]$$

The amplifier's voltage gain is determined by the following:

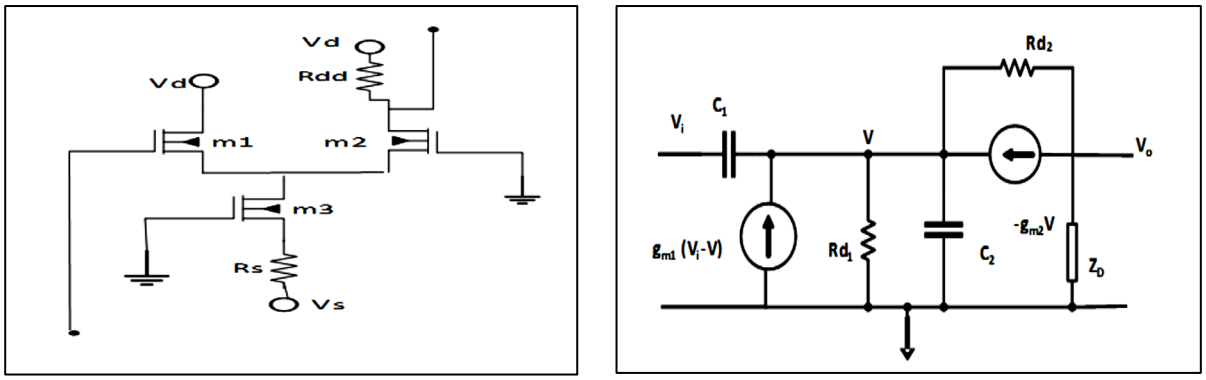
$$A = \frac{g_m (R_{og} R_{od})^{1/2} \sinh\left[\frac{n}{2}\left(A_d - A_g\right)\right] e^{-n\left(A_d - A_g\right)/2}}{2\left[1+(\omega/\omega_g)^2\right]^{1/2}\left[1-(\omega/\omega_c)^2\right]^{1/2}\sinh\left[\frac{1}{2}\left(A_d - A_g\right)\right]} \quad (4)$$

The typical impedance of gate and drain lines is R_{og} and R_{od}. If $R_{\text{og}} = R_{\text{od}} = R_o$, then the amplifier's maximum voltage gain is given by:

$$|A_v(0)| = \frac{1}{2} n g_m R_0 \quad (5)$$

4. The Proposed Matrix Differential Design

As a gain cell in distributed amplifiers, Quasi-differential amplifiers do not require a balun and can boost bandwidth. The amplification from DC, low noise, strong stability, and correct coupling and flexibility are further advantages. Figure 3(a) depicts the basic architecture of a QDA amplifier for use in a distributed amplifier system. The current source in this circuit is a transistor m_3, whereas the biased transistors are transistors m_1 and m_2. The gate of m_1 and the drain of m_2 are used to receive the input signal and deliver the output signal, respectively. The resistor Rudd is the drain load resistor of transistor M2. Its value should be high enough to increase the voltage gain of the differential stage. Figure 3(b) shows the equivalent circuit of the QDA amplifier. In Figure 3(b), resistances rd1 and rd2 are the internal (intrinsic) drain-to-source resistances of transistors m_1 and m_2, respectively. The external resistor R_{dd} is part of the drain load impedance ZD appearing in the equivalent circuit model.



(a) (b)

Figure 3: The quasi-differential amplifier (QDA) is a distributed amplifier's gain cell. (b) Equivalent circuit for the proposed QDA

The Quasi-differential amplifier's S-parameter matrix is given by:

$$[S]_{QDA} = \begin{bmatrix} 1 & 0 \\ \frac{2g_{m1}g_{m2}}{g_{m1}+g_{m2}} & 1 \end{bmatrix} \quad (6)$$

If $g_{m1} = g_{m2} = g_m$, then:

$$[S]_{QDA} = \begin{bmatrix} 1 & 0 \\ g_m & 1 \end{bmatrix} \quad (7)$$

The voltage gain of a QDA is identical to that of a conventional common source amplifier and may be calculated as follows:

$$A_V(0) \approx g_m \cdot R_o \tag{8}$$

If the system impedance is the same as the impedance of the gate and drain lines, the Quasi-differential distributed amplifiers' ports can be matched. In this instance, the artificial transmission line is lossless. Therefore, the voltage gain, also cut-off frequency, and line impedance can be determined as follows:

$$|A_v(0)| = \frac{1}{2} n g_m R_0 \tag{9}$$

$$f_{cg} = \frac{\omega_{cg}}{2\pi} = \frac{1}{\pi\sqrt{L_g C_g}} \tag{10}$$

$$Z_{gate} = \sqrt{\frac{Z_g}{Y_g}} = \sqrt{\frac{L_g}{C_g}} \tag{11}$$

Matrix Distributed Amplifier is a typical approach for achieving high gain in DAs. Strong input-output isolation ensures great stability, low harmonic factors, and oscillation in a typically distributed amplifier. Furthermore, the gain modules may be easily cascaded due to perfect input-output impedance matching. For example, if m identical amplifier circuits are connected as a matrix, the matrix gain is as follows:

$$|A_v|_{matrix} = |A_{v1}|^m \tag{12}$$

The suggested MQDDA circuit is depicted in Figure 4, with m = 4 and n = 2. The cascade connection of multiple amplifier stages requires a blocking section after each stage. The blocking section is a capacitor that will decrease the amplifier's gain in lower frequencies to zero when the frequency approaches the dc. The inserted capacitor C is called a Metal-Insulator-Metal capacitor (MIM) [27]. The flowchart of the proposed QDDA design with *n* stage is shown in Figure 5.

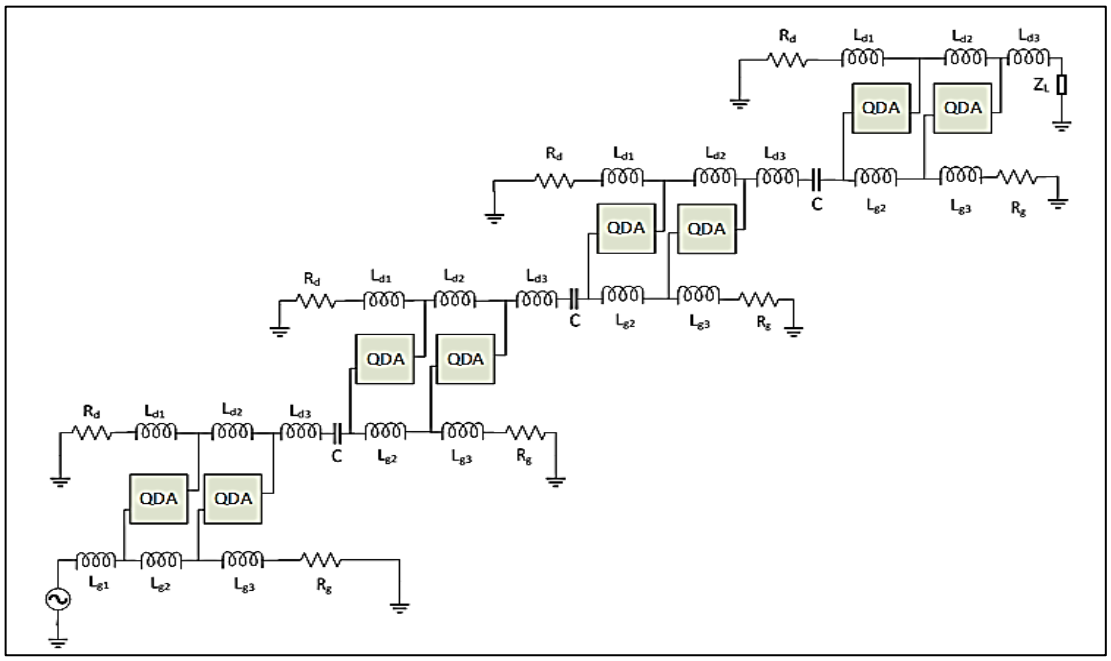


Figure 4: Schematic diagram of the proposed Matrix Quasi differential distributed amplifier

The value of $V_{c.k}$ is found to be frequency-dependent, particularly for tiny k values. The overall gain at the output has a high ripple because all node voltages contribute to the output via the FETs' transconductance. In this work, a new design technique called shifting the second tier was applied as a solution to this challenge (SST). The second tier is relocated away from the centerline's earlier nodes in this circuit, preventing amplification from these nodes. As a result, without sacrificing

total gain or bandwidth, this arrangement enhances gain–flatness. However, the shift of the second tier increases the size of the circuit due to the use of new inductances inserted in the shifted space; therefore, this improvement comes at the expense of the chip area. The total DC power consumed by the amplifier is calculated from:

$$P_{DC} = V_{DD}.I_D + V_{DD}I_S \quad (13)$$

Where ID and IS are the total DC currents consumed by sources V_{DD} and V_{SS}. These DC currents can be calculated from current probes inserted in the circuit after performing DC simulation using ADS.

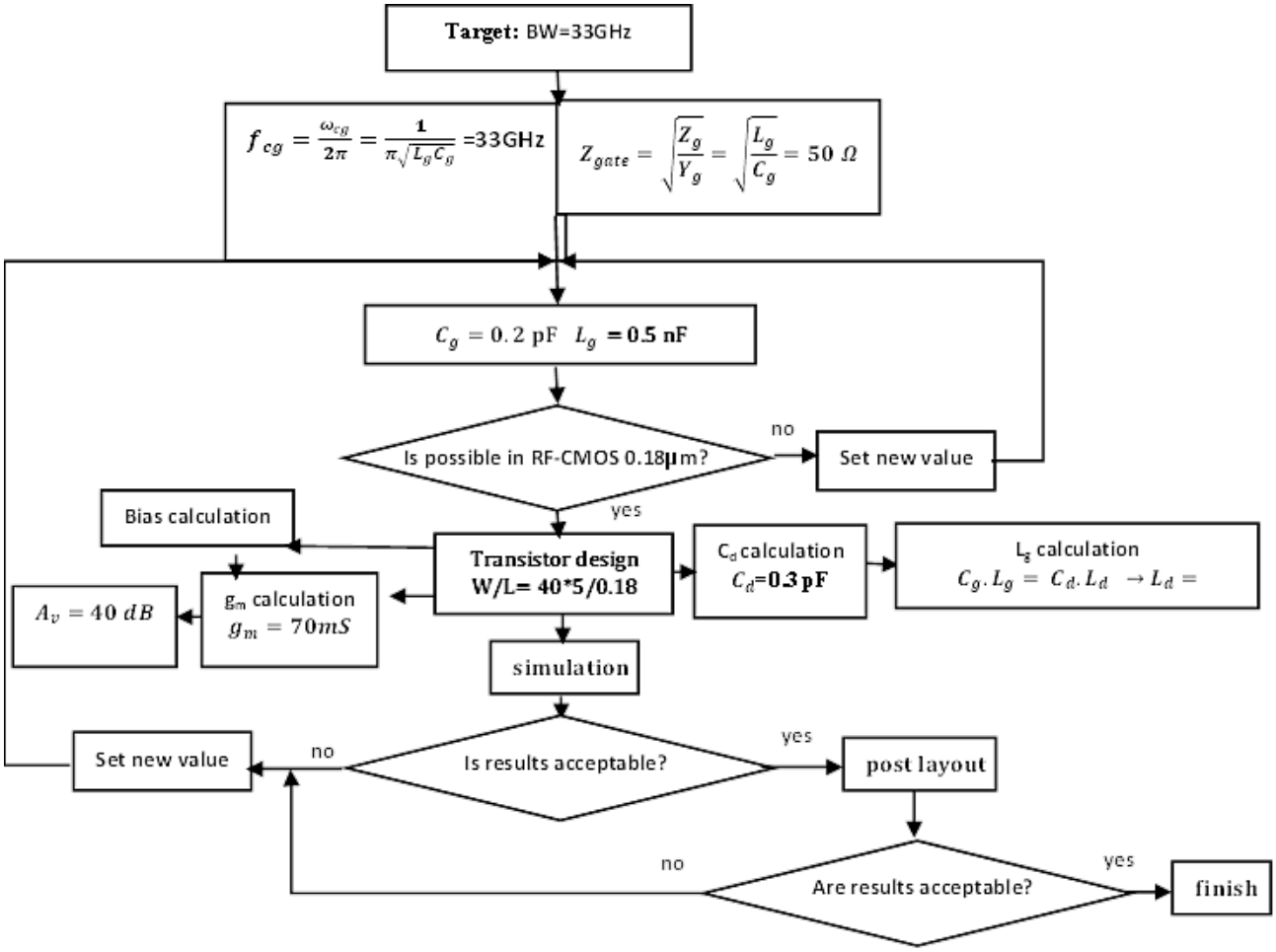


Figure 5: Flowchart for designing a QDDA with *n* stages

5. The Performance of The Proposed Amplifier

To validate The Matrix Quasi Differential Distributed Amplifier (MQDDA) suggested concept, it was compared to a traditional amplifier design Matrix Distributed Amplifier (MDA). Both circuits use the same components for the passive and active cells and have the same number of stages (three). The gain block in the MDA is made up of a single FET, whereas the QDA circuit is used in the suggested architecture. Figure 6 shows the gain response of the classical and proposed MDA. The MQDDA has more benefits in reaching higher gain and wider bandwidth and being stable and flat in the response. Table 1 shows the final component values used in the design.

Table 1: Final element values used in the design

Parameter	Value	Parameter	Value	Parameter	Value
Vd	$3.3v$	C_d	$0.3\ pF$	L_d	$0.2\ nH$
Vs	$2.8v$	C_g	0.2 pF	L_g	0.5 nF
$After\ trade\ off$:		C_g	0.2 pF	L_g	0.3 nF

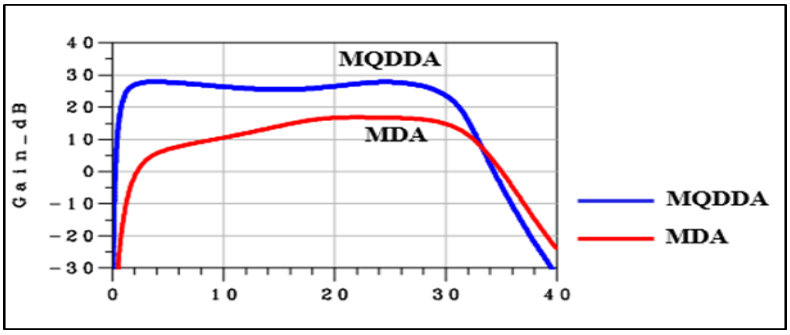


Figure 6: Gain of MDA VS MQDDA

6. Results and Discussion

The circuit design of Matrix Quasi differential distributed amplifier MQDDA demonstrates a novel MDA structure based on cascading and differential amplifiers. S-parameter analysis using ADS is used to simulate the circuit, as shown in Figure 7. In comparison to prior works stated in the linked study. The DA coefficient (S21) is 40 dB, whereas the bandwidth is from DC to 33 GHz. The power gain is approximately flat bandwidth responses and decreases rapidly after 33 GHz, as shown in Figure 7 (a). The input and output return losses are less than -10 dB, as shown in Figures 7 (b) and 7 (c). So, the design is acceptable, matching the entire frequency range. However, reverse isolation S12 is less than -40 dB Figure 7 (d). The minimum noise figure (NFmin) is shown in Figure 8(a), with the lowest value of 3.583 at 11 GHz, and the actual noise figure of the circuit versus frequency is sketched in Figure 8(b). The stability factor of the proposed design is shown in Figure 9(a), showing a stable operation over the desired band. The phase angle of S21 versus frequency is presented in Figure 9(b) to indicate the linearity of the phase response. The abrupt change in phase at 33 GHz is due to the unstable operation of the amplifier at this frequency. Also, the 1-dB gain compression point (P1dB) is about +6.4 dBm at 25 GHz, as shown in Figure 10. It could be noted the (P1dB) will decrease as the frequency increases. The amplifier's final layout is presented in Figure 11, and the MQDDA layout demonstrates that the suggested approach has also enhanced GBW. The implemented chip is 1.132 mm^2 size when the pads are included. Off-chip capacitors and chokes are used in the bias circuit.

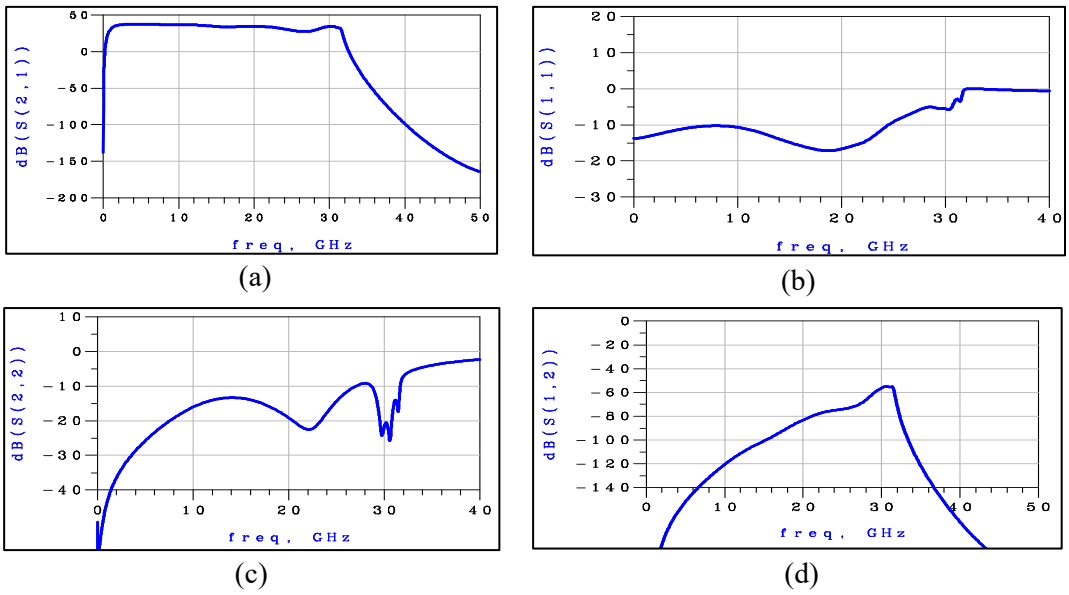


Figure 7: The S-parameters of the proposed MQDDA. (a) S21, (b) S11, (c) S22 and (d) S12

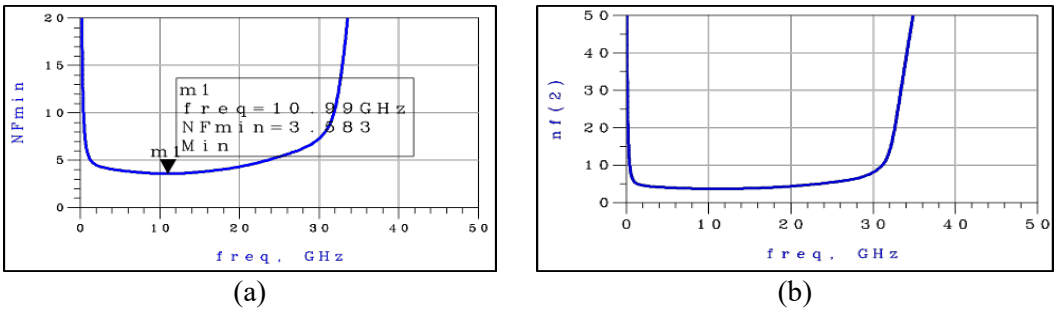
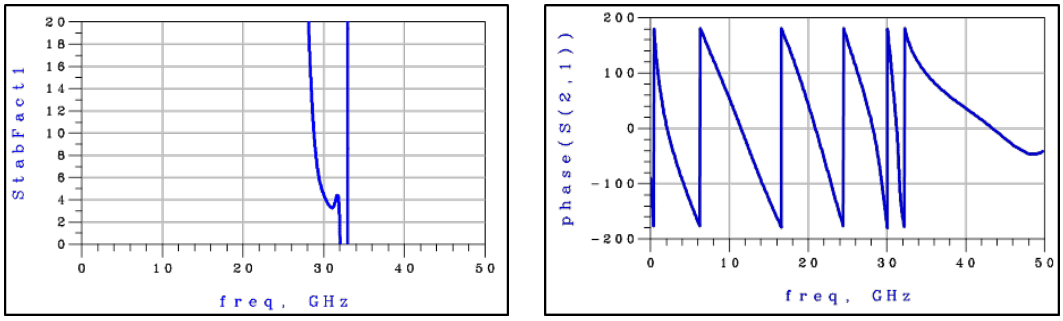


Figure 8: (a) The minimum NF of the proposed MQDDA. (b) The actual NF of the proposed MQDDA



(a) (b)

Figure 9: (a). The stability factor of the proposed MQDDA. (b) The phase angle of S_{21} versus frequency

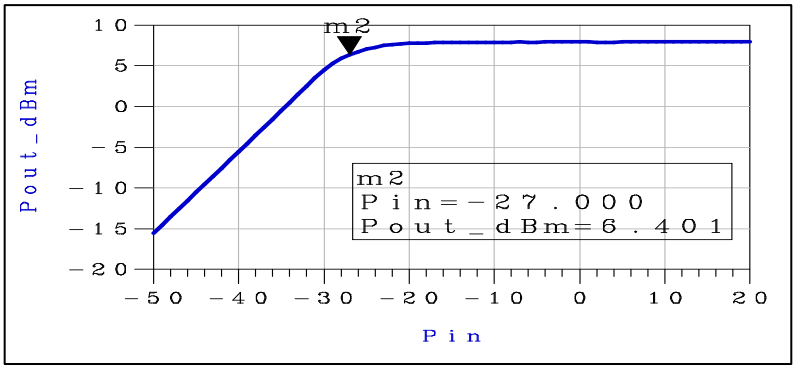


Figure 10: The 1-dB gain compression point@25GHz (P_{1dB}) of proposed MQDDA

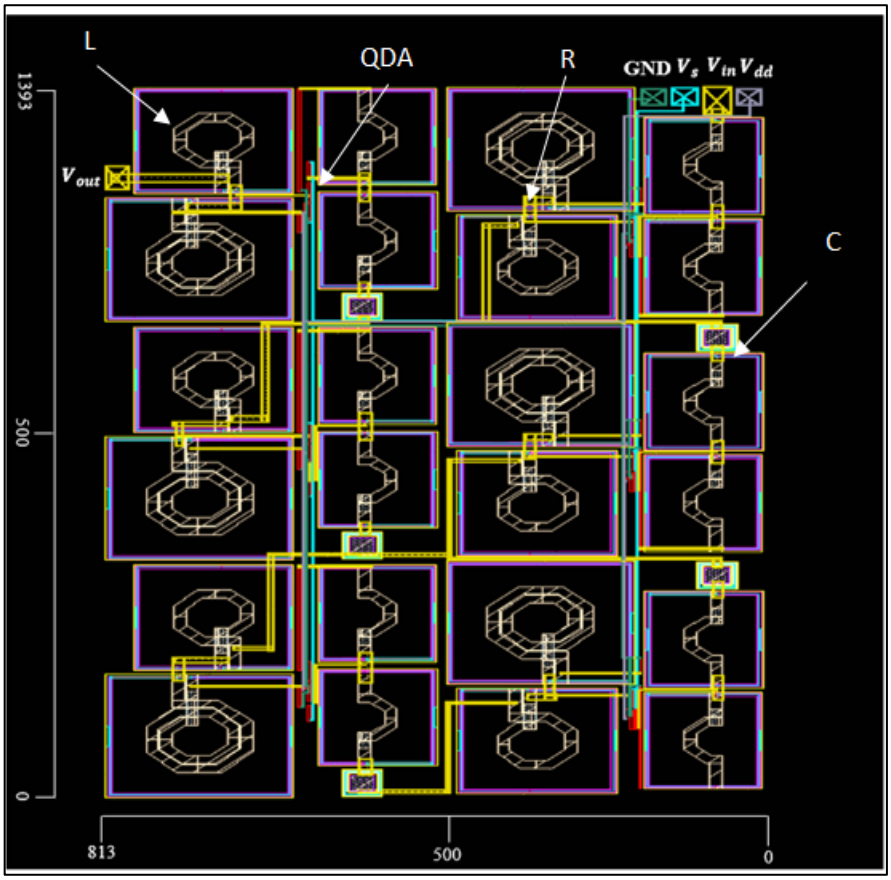


Figure 11: Die Micrograph of the proposed MQDDA

Table 2 shows an overview of the implemented CMOS DAs and state-of-the-art CMOS DAs wideband LNAs that have recently been described based on the distributed amplifier structure. However, distributed amplifiers with high gain, outstanding linearity, and average NF advantages can be shown over other architecture. Therefore, the suggested roll-off problem on MQDDA architecture will be more obvious if CMOS technology is adopted.

Table 2: Summary of previous works on DAs and the results of current work

Gain (dB)	BW (GHz)	GBW (GHz)	NF (dB)	Ripple (dB)	Area (mm^2)	Technology	Ref.
15	12.5	70	_	±2	5.8	0.18 µm CMOS	[13]
7.1	16	36	4.1	±2	2.02	0.13 µm CMOS	[14]
20	324	3240	_	±1	_	_	[15]
12	19.5	78	5-6.75	±1	-	0.18 µm CMOS	[28]
11.6	7.9	30	3.55-4.25	±0.6	2.16	pHEMT	[29]
40	33	3300	3.583	±1	1.1	0.18 µm CMOS	This work

7. Conclusion

The MQDDA proposed a decent solution to the gain bandwidth roll-off problem. In 0.18m, CMOS technology with MQDDA was developed and tested. Due to the greatest cut-off frequency of the Quasi-differential amplifier, the QDA design technique was used for adopting the distributed amplifier design. This means increasing the bandwidth by using differential amplifier cells substituted by increasing the number of stages. Therefore, the best performance is achieved by designing the QDDA using the QDA. The suggested (MQDDA) 1.1 mm^2 layout area is a decent and acceptable value compared to other works. The average gain of the MQDDA is 40 dB with a bandwidth of 33 GHz. The measured results revealed that the MQDDA design is decreasing the roll-off problem in which the values of gain and bandwidth are approximately balanced (High gain and high bandwidth). The advantage of low manufacturing cost has been made by CMOS technology widely used in microwave applications. Future works, based on other techniques such as InP, might enhance the bandwidth instead of CMOS.

Author contribution

All authors contributed equally to this work.

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Data availability statement

The data that support the findings of this study are available on request from the corresponding author.

Conflicts of interest

The authors declare that there is no conflict of interest.

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