Represent Different Types of Sliding Mode Controllers by VHDL

Yousra Abd Mohammed^{*} Dr. Ekhlas H. Karam ** & Mohammed H. Khudair** *

Received on:28/4/2008 Accepted on:7/5/2009

Abstract

This paper focus on represent and implementation the conventional sliding mode control (SMC), in addition to some types of the common enhancement SMC approaches using reconfigurable hardware technology based on Field Programmable Gate Arrays (FPGAs); this is because FPGAs are highly attractive options for hardware implementation. The enhancement SMC approaches that used here are:1) the conventional SMC with boundary layer, 2) PI sliding mode controller, and 3) boundary SMC with new approximation sign function. The main key of this work is to implement these SMC approaches in high volume FPGA devices, a low area and fast clock speed device, where these approaches are implemented in Xilinx Vertix family Xcv1000-fg680-4 FPGA (the occupation rate is 86% and maximum net delay is 0.032 ns). All the architectures in VHDL, verified the functionality using Active-HDL simulator, and synthesis the data paths using ISE 4.1i software package synthesis tool and Xilinx place and route tool of this package. Finally, to test the performances of the enhancement SMC approaches, computer simulation is performed on linear and nonlinear system models in order to compare the performance of these SMC approaches to illustrate which approach between them give more efficient performance than the others.

Keywords: Conventional SMC, enhancement SMC, VHDL, linear and nonlinear systems.

(Sliding mode controllers) تمثيل أنواع مختلفة من مسيطرات الطريقة المنزلقة (VHDL) بلغة الوصف المادي (VHDL)

الخلاصة

هذا البحث يركز على تمثيل وتطبيق سيطرة النمط المنزلقة التقليدية (SMC) , بالاضافة الى بعض ألانواع من الطرق المحسنة الشائعة لمسيطرات النمط المنزلقة (Sliding mode) بأستخدام تقنية برمجة واعادة برمجة الماديات مستندة على رقاقة المصفوفات المبرمحة (FPGA) , وذلك بسبب ان هذه الرقاقات هي خيارات جذابة جدا" لتنفيذ الكيان المادي الهدف الاساسي من هذا البحث هو تنفيذ أربعة أنواع من المسيطرات نوع (Sliding mode)

2494

https://doi.org/10.30684/etj.27.12.18

2412-0758/University of Technology-Iraq, Baghdad, Iraq

This is an open access article under the CC BY 4.0 license http://creativecommons.org/licenses/by/4.0

بأستخدام ال (FPGA) وذلك لغرض المساحة القليلة والسرعة العالية للتنفيذ في هذا العمل قد تم استخدام رقاقة المصفوفات البرمجية نوع (Active-HDL) بحيث كانت نسبة المستخدم من هذه الرقاقة هو 86% وتأخير صافي أقصاه ns 0.032 ولغرض التأكد من الاداء الوظيفي بصورة صحيحة للمسيطرات فقد تم أجراء المحاكاة الوقتية (Timing Simulation) باستخدام برنامج ال (Active-HDL simulator) ولاكمال باقي العمليات التنفيذية (ISE 4.11) وأخيرا ولغرض تجيك عمل هذه المسيطرات, انجزت عدة محاكاة حاسوبية على نماذج لأنظمة خطية وغير خطية بأستخدام برنامج ال (Mat. Lab.)

Introduction

Sliding Mode Control (SMC) is a technique derived from Variable Structure Control (VSC) which were discussed first in the Soviet literature [1, 2], and have been widely developed in recent years. Comprehensive surveys of variable structure control can be found in [3, 4]. SMC is often favored basic control approach, especially because the insensitivity property toward the parametric uncertainties and the external disturbances [5].

SMC are characterized bv control laws that are discontinuous on a certain manifold in the state space, the so-called sliding surface [2, 6]. The control law is designed such representative point's that the trajectories of the closed-loop system are attracted to the sliding surface and once on the sliding surface they slide towards the origin [7]. However the major drawback in the SMC approach is the undesired phenomenon of because chattering of the discontinuous change of control laws across the sliding surface. In practical engineering systems, chattering may cause damage to system components, as well as excite unmodelled and high frequency plant dynamics [8].

There exist several techniques to eliminate chattering. The widelyadopted approach to chattering-free VSC is the so-called boundary layer, where the discontinuous VSC control law signum function is applied to a small vicinity around the sliding surface (see [4, 9]). Unfortunately, boundary layer controllers do not guarantee asymptotic stability but rather uniform ultimate boundedness [10]. As a consequence, there exists a trade-off between the smoothness of control signals and the control accuracy. Some boundary layer width modification techniques to improve tracking precision are discussed in [9, 11]. Nevertheless, these proposed methods in practice lead to a computational burden when implemented, or are applicable only to linear systems [7].

Another solution to chattering problem is to attempt to smooth the signum function to obtain a continuous approximation. The signum function is seen to be relaylike in nature. The ideal relay characteristic is often impossible to implement. One possible answer is to

replace the signum function by a sigmoid-like function to induce pseudo-sliding instead of ideal sliding [12]. In some cases, the control signal is thought to comprise of 'low' and 'high' frequency components. A natural solution is to pass the discontinuous control signal through a low pass filter to eliminate the high frequency component in the control signal[13]. Using higher order sliding modes(HOSM) is another possible solution to the chattering problem [13]. This paper aims to present the some of the common approaches that provide an effective way to resolve the chattering problem. All these approaches are of fixed structure then implement these approaches in addition to the conventional SMC with the FBGA technique to become easy use with different control The paper is organized as systems. follows. In section II un introduction to FBGA technique is presented. In section III some basic concepts of the SMC approach is given. In section III, the enhancement approaches of SMC will be presented in section IV and implemented with FBGA platform in section V. In section VI we will show several computer simulation results of the SMC approaches. Finally, conclusions are drawn in section VII.

II. Field Programmable Gate Array and VHDL

FPGA: The Field-Programmable Gate Array (FPGA) places fixed cells on the wafer, and the FPGA designer constructs more complex functions from these cells. However, the cells provided on the FPGA can be Represent Different Types of Sliding Mode Controllers by VHDL

substantially more complex than the simple gates provided on the gate array. In addition, the term *field* programmable highlights the customizing of the IC by the user, than by rather the foundry manufacturing the FPGA [14]. Several different types of structures for **FPGAs** are available commercially. All of them have a basic structure that consists of many blocks logic logic or cells. accompanied by a large number of pre-laid lines for connecting these logic blocks. [15].Depending on the FPGA type, special-purpose structures are placed into the array. Most often, these are configurable RAM blocks and clock distribution elements. multipliers, adders, etc. Around the periphery of the chip are the I/O cells, which commonly contain one or more flops to enable high-performance synchronous interfaces [16].

Field Programmable Gate Array (FPGA) is an integrated circuit that can be bought off the shelf and reconfigured by designers themselves. With each reconfiguration, which takes only a fraction of a second, an integrated circuit can perform a completely different function. From several FPGA families available on the market, we have chosen the high performance Virtex family from Xilinx, Inc. [17]. FPGA devices from this family consist of thousands of universal building blocks, known as Configurable Logic Blocks (CLBs), connected using programmable interconnects, Reconfiguration is able to change a function of each CLB and

connections among them, leading to a functionally new digital circuit [17].

VHDL: The acronym VHDL stands for the VHSIC Hardware Description Language. The acronym VHSIC, in turn, refers to the Very Speed Integrated High Circuit program. [18]. VHDL is a language for describing digital systems at many levels of abstractions ranging from the algorithmic level to the gate level [19]. Such description can be used by a simulator for simulating the behavior of the system without having to actually construct the system. Alternative synthesis compiler can utilize such a description for creating description of the digital hardware for implementing the system [20].A circuit or subcircuit described with VHDL code is called a *design entity*, or just entity. It has two main parts: the entity declaration and the architecture [21]. In VHDL an entity is the equivalent of an IC package in electronics. A package is defined by its name and the number and nature of ports it used to exchange data and interact with external circuits. It is not relevant to the function that the component performs, the resources it uses, or the complexity by which it is characterized [22]. Architecture, continuing with the analogy of an IC, is equivalent to the internal electronic circuit that performs the function for which the component has been designed. At this stage all the signals the entity uses to communicate with the external world are defined and unchangeable [23].

III. Basic Concepts on Sliding Mode Control

The first step in SMC is to define a time-varying sliding surface S(t) that is linear and stable. Three S(t) acting on the tracking-error expression are selected in this work, these sliding surfaces are:

1) derivative-differential equation which is defined as:

$$S(t) = l e(t) + \mathscr{U}(t)$$
 ...(1)

2) integral-differential equation that is defined as:

$$S(t) = e(t) + I_{i} \int_{0}^{t} e(t) dt \quad ..(2)$$

3) derivative-integral-differential that is defined as:

$$S(t) = Ie(t) + \mathscr{U}(t) + I_{i} \int_{0}^{t} e(t) dt \dots (3)$$

where l, l_i are a strictly positive constant, and $e(t) = r_d(t) - y(t)$ is the tracking errors, the $r_d(t)$ is the desired input (setpoint) and y(t) is the output measurement (state). while $\mathcal{R}(t)$ is the time derivative of the tracking error e(t) and $(\int_{0}^{t} e(t) dt)$ is an

integration term to reduce the system steady state error.

Sliding mode means that once the state trajectory *e* has reached the sliding surface S=0 the system trajectory remains on it while sliding into the origin *e*=0, independently of model uncertainties, unmodeled frequencies, and disturbances [24]. By choosing the Lyapunov function candidate:

$$V = \frac{1}{2} S(t)^{T} S(t) \ge 0 \quad ...(4)$$

and depending on the time derivative for the above Equation, a reaching condition (sliding condition) is obtained as;

$$S(t)^T \mathscr{S}(t) \leq -h|S(t)|$$
(5)

where h is a positive constant that guarantees the system trajectories hits the sliding surface in a finite time.

Equation(5) provides a sufficient reaching condition such that the tracking error e(t) will asymptotically converge to zero [25]. In order to meet that condition, the control law u of Fig. 1 is chosen as follows

$$u = K \operatorname{sgn}(S) \qquad \dots (6)$$

where the sliding gain K>0 and sgn(S) is a sign(or signum) function, which is defined as

$$\operatorname{sgn}(S) = \begin{cases} -1 & \text{if } S < 0\\ 0 & \text{if } S = 0\\ 1 & \text{if } S > 0 \end{cases} \dots (7)$$

As explained before, using a sign function often cases a chattering problem. In the next section different enhancement sliding mode control(ESMC) approaches that used for avoided or reduce chattering problem are presented and implemented with FBGA technique.

IV. Different ESMC Approaches

In this section, three SMCs are given, the first and the third approach of these will explained for the sliding function of Eq.(1), while the second

Represent Different Types of Sliding Mode Controllers by VHDL

one will explained with the sliding function of Eq.(3), but we can use any sliding function with these controllers as will given in next sections. However these approaches are:

IV.1 SMC with Boundary Layer

Slotine [4] proposed a technique to change the dynamics near to the sliding surface in order to avoid a real discontinuity and at the same time to preserve the sliding mode properties. This technique introduces boundary layer(BL) on both sides of the sliding surface in order avoid the chattering effect in the control signal. The thin BL neighboring the sliding surfaces is defined as [24];

$$B(t) = 2\Phi, \quad \Phi > 0 \quad \dots \dots (8)$$

where Φ is the boundary layer thickness, let |S| is the distance between state *e* and sliding surface S=0. Then a state *e* is located inside the BL if $|S| \le \Phi$, and it is located outside if $|S| > \Phi$, see Fig. 2, to remedy the control discontinuity in the boundary layer, the signum function (sgn(S)) is replaced by a saturation function, see Fig. 3 of the form [2].

$$sat(S) = \begin{cases} sgn(S), & if |S| \ge \Phi \\ \frac{S}{\Phi}, & if |S| < \Phi \\ \dots \dots (9) \end{cases}$$

Although, the sliding variable will reach within the vicinity of the sliding surface. However, the accuracy and robustness of the sliding mode are

partially lost [5]. Let $e = l^{-1}\Phi$, be the boundary layer width. As shown in [6], the tracking errors exist within a guaranteed precision e. Therefore, the larger the boundary layers the smaller the control chattering and the greater the tracking errors [2].

IV.2 PI Sliding Mode Controller

A proportional-integral combination of the sliding function is proposed in the boundary layer in place of the signum function by [7]. This continuous controller can force the system states to reach the sliding surface and attain high tracking performance. The equation for this saturated proportional-integral functions is given by [7];

$$r_{p_{I}}(\boldsymbol{S}_{p_{I}}) = \begin{cases} 1 & \text{if } \boldsymbol{S}_{p_{I}} > 1 \\ \boldsymbol{S}_{p_{I}} + \boldsymbol{K}_{I} \int_{t_{i_{0}}}^{t_{i_{1}}} \boldsymbol{S}_{p_{I}} & \text{if } -1 \leq \boldsymbol{S}_{p_{I}} \leq 1, \\ -1 & \text{if } \boldsymbol{S}_{p_{I}} < -1 \\ & \dots(10) \end{cases}$$

where $\boldsymbol{S}_{PI} = \frac{S}{\Phi}; \quad K_I > 0$ is an

integral gain, and t_{i0} is the initial time when the system states enter the boundary layer B(t) in Eq.(8). If $|\mathbf{s}_{pl}| \ge 1$ the integration term in Eq.(10) will be reset to zero to prepare for the system state entering boundary layer. It is assumed that the chosen integration gains K_l are sufficiently large such that Represent Different Types of Sliding Mode Controllers by VHDL

 $\begin{aligned} \mathbf{s}_{p_{l}} + K_{l} \mathbf{s}_{p_{l}} > 0 & \text{for all } \mathbf{s}_{p_{l}} > 0 \\ \mathbf{s}_{p_{li}} + K_{l} \mathbf{s}_{p_{l}} < 0 & \text{for all } \mathbf{s}_{p_{l}} < 0 \\ & \dots (11) \end{aligned}$

Inequalities (11) imply that r_{p_I} increases for all $s_{p_I} > 0$, and r_{p_I} decreases for all $s_{p_I} < 0$ [26].

IV.3 Boundary SMC with New Approximation sign Function

The sliding function of Eq.(3) is used in this section and in order to reduce the chattering effect in the SMC and to avoid simulation difficult, the function in Eq.(12)[11, 27] has been used to approximate the sign function(sgn(S)) of Eq.(7);

$$\operatorname{sgn}_{a}(S) \approx \frac{S}{|S| + d_{s}}$$
(12)

where d_s is a small positive constant, and can be used to trade-off between maintaining ideal performance and obtaining smooth control action[13], in this case the saturation function of Eq.(9) becomes

V. Proposed FPGA Design and Implementation of Sliding Mode Controllers

The proposed design in field programmable gate arrays as shown in Fig.4 is divided into four components; each component is represented one

type of sliding mode controllers (SMCs) as shown in the following points:

1- SMC1: is represented the conventional SMC.

2- SMC2: is represented SMC with boundary layer.

3- SMC3: is represented PI sliding mode controller.

4- SMC4: is represented the boundary SMC that have new approximation sign function.

Each of these controller works independent of others, so the user is decided which controller is done depending on controller chip select as shown in Table(1), this table shows how the user can be selected any of these four types of controllers; so when the chip select pins S2 S1(2-bit vector signal) equal to (00) this leads that the signal (EN1) is active so that the first type of these controllers (general SMC) is selected; but when (S2 S1)=10, i.e. (EN2) is active ,therefore the second controller (SMC with boundary layer) is selected and so on. There are three types of sliding function (S(t)) to this proposed SMCs design, in order to chose which of these three inputs is active (implemented); there is a sliding function chip select inside each of these four controllers, the inputs to this chip is SF (2-bit vector signal) and the output is FI (3-bit vector signal); therefore any of sliding equations is implemented as shown in Table (2). The signal FI=001 by the assertion of SF to 00, so Eq.(1) is implemented; but when SF=01,

FI=010, therefore Eq.(2) is Implemented, finally Eq.(3) is implemented when SF=10 that means FI=011.

The final output (control action) of the proposed FPGA sliding mode controllers design is determined by the output chip select, inputs to this chip are the four enable signals of controller chips select (EN1.EN2.EN3.and EN4) and the output control action of each controllers (U1,U2,U3,and U4). The output of the output chip select is only the control action of the chosen working controller according to enable signals as demonstrated in Table(3). The design and implementation operation of this proposed FPGA design is done by using ISE 4.1i package based on VHDL language (combination of structural and behavioral architecture) and Xilinx Vertix family (Xcv1000fg680-4) FPGA as hardware device; so the design become more reliable and adaptable for future developments.

The functionality behaviors of these controllers are verified using timing simulation tools of Active-HDL program, therefore some of simulation results are presented in this paper as shown in Figs. from 5 to 11. Synthesis, map, and timing constraint reports are shown in Figs.12, 13, and 14.

Finally to show how the final FPGA design of the sliding mode controllers works, take for examples Fig. 5 and Fig. 6 for behavioral simulation. In Fig. 5 for λ =c=2, k=10 and by the assertion of these signals

((S = (S2S1) = 00) and SF=00), this lead to 4-bit enable vector (EN) equal to 0001 that mean EN1 is active and FI=001, therefore the first type of controllers is selected and implemented the first sliding function equation for different values of error (*e*) and change of error (*ce*), so the control action (u) is the output of the first controller(general).

In Fig. 6 for 3=c=1, k=10, $\Phi=f=0.5$, S2S1=01 and SF=00, this lead to 4-bit enable vector (EN) equal to 0010 that mean EN2 is active and FI=001, therefore the second type of controllers (SMC with boundary layer) is selected and implemented the first sliding function equation for different values of error (*e*) and change of error (*ce*), so the control action (*u*) is the output of the second controller.

VI. Simulation Results

In this section and with Matlab Simulink (version 7.0 and R2006a), we show some computer simulation results using the ESMC approaches that presented in this paper. In these simulations, several linear and nonlinear systems are tested (taken from ref.[28]) in addition to linear unstable and linear time varying examples (these two examples are presented in Appendix B) to illustrate the performance of the these methods for step or ramp or parabolic reference inputs, and also to show which between approach them give remarkable performance, as good as (if not better than) the other approaches, while the simulation results for these systems with unity feedback (without controller) and with conventional SMC are given in the Appendix A (see this Appendix A). For simplicity, we refer to the first ESMC approach(SMC with boundary E1-SMC, The second layer) as ESMC (PI-sliding mode controller) as E2-SMC, while the third one (boundary SMC with new approximation sign function) is refer as E3-SMC, note that this controller $d_{c} = 0.05$ for all the tested use systems.

A. Linear Models

Two second-order linear systems examples have been tested; the first example is a system with the transfer function

$$G(s) = \frac{2}{s^2 + 4s + 3} \qquad \dots (14)$$

Suitable control parameters that satisfy Eq.(5) are selected for each SMC approach, these parameters are given in Table(4), we refer to the parameter that is not used as "---". This table also shows the type of the sliding function that is used by these controllers. If the unit step input $(r_d(t)=1)$ is used, then the response of the close loop system (without SMC or any controller) for the above plant will track the desired input without oscillation but with steady state error more than 40% (see the appendix), where the steady state error is calculated by;

$$e_{ss} = \lim_{t \to \infty} e(t) \qquad \dots (15)$$

But, if ESMC approaches are used to control this system (see output, error and control signal form Fig.15), then it clearly reveals that the system with

Represent Different Types of Sliding Mode Controllers by VHDL

all the ESMCs track the input without any oscillation but with steady state error less than 0.6%, 0.8%, and 2.26% for E2-SMC, E3-SMC, and E1-SMC in respectively, that mean the E2-SMC and E30-SMC are given better the performance than E1-SMC although it use smaller boundary thickness ($\Phi = 0.2$) than the other. Furthermore, it is obvious from these results that all ESMCs regulate the system with remove the chattering from the control comparing with conventional SMC which suffer from this problem.

The second linear example has the following transfer function.

$$G(s) = \frac{1}{s(s+100)}$$
 ... (16)

Which is only marginally stable, the sliding functions and the control parameters that used for this example are given in Table(5). If reference is parabolic signal $r_{\rm d}(t)=0.15t^2$, then results are shown in Fig.16. This table shows that all the SMCs use the sliding function of Eq.(2). We observed from Fig.16a, that all the SMCs approaches are able to track the parabolic signal, it is also clearly reveals from Fig.16b that the E2-SMC has less than 0.0072% steady state error, and the steady state error with E1-SMC and E3-SMC is less than 0.738% and 0.753% in respectively, which mean that the performance of E1-SMC and E3-SMC is same but since E1-SMC use $I_i = 5.1$ this make the steady state error became smaller than the E3-SMC.

Fig. 16c shows that the control signals of E1-SMC and E2-SMC are smooth more than the control signal of E3-SMC.From the above linear examples, it is easy to conclude that all the performance of ESMCs is remarkable especially E2-SMC, this is because the structure of it contain the integral term K_I that help to improve the performance of it, therefore it has steady state error less than E1-SMC and E3-SMC.

B. Nonlinear Models

Two examples are chosen here for simulation and comparison, as mention in above these examples are taken from [28]. The first nonlinear example has the following simple mathematical model:

$$\mathfrak{K}(t) = 0.0001 |y(t)| + u(t)$$
 ... (17)

For ramp input and controller parameters given in Table (6), this table show that all the ESMCs use the sliding function of Eq.(2), The simulation results are given by Fig. 17. we observed from these results that all the SMCs approaches produce faster convergence rate to the desired ramp input without chattering and with smaller error comparing with the conventional SMC, see the appendix to show the difference between these controller. Finally the enhancement SMC approaches have been compared by using a another nonlinear example model from [28], this model is described by;

$$\mathfrak{K}(t) = -y(t) + 0.5y^2(t) + d(t) + u(t)$$

....(18)

The controller parameters are given in Table(7), this table show that E1-SMC and E2-SMC use the sliding function of Eq.(1), while E3-SMC use the sliding function of Eq.(2). However, the simulation results of such system for unit step input $r_d(t)=1$ are shown in Fig. 18,

The simulation results demonstrate one again that all the ESMCs enhance the performance of the simulated example than the conventional SMC spatially the E2-SMC, where all SMCs produce a good tracking response, and they are effective for eliminating chattering even in the presence of noisy disturbance specially by E2-SMC which achieved steady state error less than 0.1%, while E1-SMC and E3-SMC achieved 3.57%, 0.5% error steady state in respectively.

From the simulation results of the above linear and two nonlinear examples, it can be concluded that the system response with all the ESMCs give efficient results esptially the E2-SMC which perform steady state error more smaller than the other approaches due to the integral part K_I in structure of it.

VII. Conclusions

This paper aims to present and implement some of the common enhancement approaches that provide an effective way to resolve the chattering problem, in addition to the conversional SMC with the FPGA technique to become easy use with different control systems, this is because FPGA provide a low area cost, speed and easy development. Computer simulation is performed on linear and nonlinear systems using Matlab Simulink version 7.0 and R2006a, the results from these simulations show that all enhancement SMC approaches that have used in this paper are able to track the desired input with no or small chattering, and with zero or small steady state error spatially the PI sliding mode controller. References

- [1] S. Emelyanov: "Variable Structure Control Systems"; Moscow: Nauka, 1967.
- [2] V. Utkin:" Sliding Modes and Their Application in Variable Structure Systems"; Moscow: Nauka, In Russian, 1974.
- [3] R. A. DeCarlo, S.H Zak, and G.P. Matthews: "Variable Structure Control of Nonlinear Multivariable Systems: a Tutorial"; Proceeding of IEEE, Vol.76, No.3, pp.212-232, Mar. 1988.
- [4] J. Y. Hung, W. Gao, and J. C. Hung: "Variable Structure Control: a Survey"; IEEE Transactions on Industrial Electronics, Vol.40, No.1, pp.2-22, Feb. 1993.
- [5] Utkin, V.I.:" Sliding Modes in Control and Optimisation", Springer-Verlag, 1981.
- [6] Y. Itkis: "Control Systems of Variable Structure"; New York, Wiley, 1976.

Represent Different Types of Sliding Mode Controllers by VHDL

- [7] T. V. M. Nguyen, Q. P. Ha and H. T. Nguyen;" A Chattering-Free Variable Structure Controller for Tracking of Robotic Manipulators"; Faculty of Engineering, University of Technology, Sydney, 2003.
- [8] H. G. Kwatny and T. L. Siu; "Chattering in Variable Structure Feedback Systems"; in Proc. IFAC 10th World Congr., vol. 8, pp. 307-314, 1987.
- [9] J.J.E. Slotine and W. Li:" Applied Nonlinear Control"; Englewood Cliffs, NJ, Prentice Hall, Englewood cliff, New Jersey, 1991.
- [10] M. Corless and G. Leitmann: Feedback "Continuous State Guaranteeing Uniform Ultimate Boundedness for Uncertain Systems"; Dynamic IEEE Transactions on Automatic Control, Vol. 26, pp. 89-94, Oct. 1981.
- [11] M. Chen, Y. Hwang, and M. Tomizuka, "A State-Dependent Boundary Layer Design for Sliding Mode Control ", IEEE Transactions on Automatic Control, Vol. 47, No. 10, pp. 1677-1681, Oct. 2002.
- [12] Edwards C.and Spurgeon S.K.; " Sliding Mode Control: Theory and Applications"; Taylor&Francis, UK, 1998.
- [13] Goh, K.B.; Dunnigan, M.W.; Williams, B.W. "Robust

Chattering-Free (Higher Order) Sliding Mode Control for a Vector-Controlled Induction Machine"; Control Conference, 2004.5thAsian, Vol. 2, Issue, 20-23, pp. 1362 – 1370, July 2004.

- [14] R. C. Dorf: "The Electrical Engineering Handbook"; CRC Press LLC, 2000.
- [15] I. W. Chen: "The VLSI Handbook"; CRC Press LLC, USA, 2000.
- [16] M. Balch: "Complete Digital Design"; McGraw-Hill companies Inc., USA, 2003.
- [17] Xilinx, Inc.: "Virtex 2.5 V Field Programmable Gate Arrays"; available at <u>http://www.xilinx.com</u>.
- [18] Z. Navabi: "VHDL: Analysis and Modeling of Digital Systems"; McGrow-Hill Companies, Inc., 1993.
- [19] J. BHASKER: "A VHDL Primer"; Prentice-Hall, Inc., Third Edition, 1999.
- [20] M. Zwolinski: "Digital System Design with VHDL"; Prentice-Hall, Inc., 2000.
- [21] S. Brown and Z. Vranesic: "Fundamentals of Digital Logic with VHDL Design"; McGrow-Hill Companies, Inc., 2000.
- [22] S. Sjoholm and L. Lindh: "VHDL for Designers"; Prentice-Hall, Inc., 1997.

- [23] Peter J. Ashenden: "The VHDL Cookbook"; First Edition, July 1990.
- [24] R. Palm, D. Driankov and H. Hellendoorn:" Model Base Fuzzy Control: Fuzzy Gain Schedulers and Sliding Mode Fuzzy Controllers"; Springer-Verlag Berlin Heidelberg, 1997.
- [25] N. H. Quang:" Robust Low Level Control of Robotic Excavation"; Ph.D., Thesis, Australian Centre for Field Robotics, University of Sydney, and Mar. 2000.
- [26] S.L. Salas and E. Hill:" Calculus: One and Several Variables"; New York: Wiley, 1990.
- [27] Oscar Camacho, Rubén Rojas, Luís González:" Sliding Mode Control Proposal for Variable Dead Time Processes"; Rev. INGENIERÍA UC. Vol. 11, No 3, Dec. 2004.
- [28] Heidar A.Malki, Huaidong Li. And Guanrong Chen,:"New Design and Stability Analysis of Fuzzy Proportional-Derivative Control Systems"; IEEE Transactions on Fuzzy Systems, Vol. 2, No.4, pp. 245-254, Nov. 1994.

Eng. & Tech. Journal, Vol. 27, No.12, 2009 Represent Different Types of Sliding Mode

Controllers by VHDL

SMC type

E1-SMC

E2-SMC

E3-SMC

Tabl	Fable (1) Sliding mode controllers select.					
S1	S2	EN1	EN2	EN3	EN4	
0	0	1	0	0	0	
1	0	0	1	0	0	
0	1	0	0	1	0	
1	1	0	0	0	1	

K

400

400

400

Table (2) Sliding function select.				
SF	FI	Note		
00	001	S(t)=Eq.1		
01	010	S(t)=Eq.2		
10	011	S(t)=Eq.3		

Table(3) Control actions of SMCs select.

U	EN1	EN2	EN3
U=U1	1	0	0
U=U2	0	1	0
U=U3	0	0	1
U=U4	0	0	0

Table (4): Example(1) parameters.

SMC type	K	Φ	I_{i}	K _I	1
E1-SMC	6.5	0.2			2
E2-SMC	6.5	0.5		0.3	2
E3-SMC	6.5	0.5	0.15		2

Table (6): Example (3) parameters.					
SMC type	K	Φ	I_{i}	K _I	1
E1-SMC	8	0.5	0.1		
E2-SMC	8	0.5	0.1	0.1	
E3-SMC	8	0.5	0.2		

Table(5): Example(2) parameters.

Φ

0.5

0.5

0.5

 I_i

5.1

5

5

 K_I

1

1

Table (7): Example (4) parameters.

SMC type	K	Φ	I_{i}	K _I	1
E1-SMC	2	0.5			3.5
E2-SMC	2	0.5		0.122	3.5
E3-SMC	2	0.5	0.3		

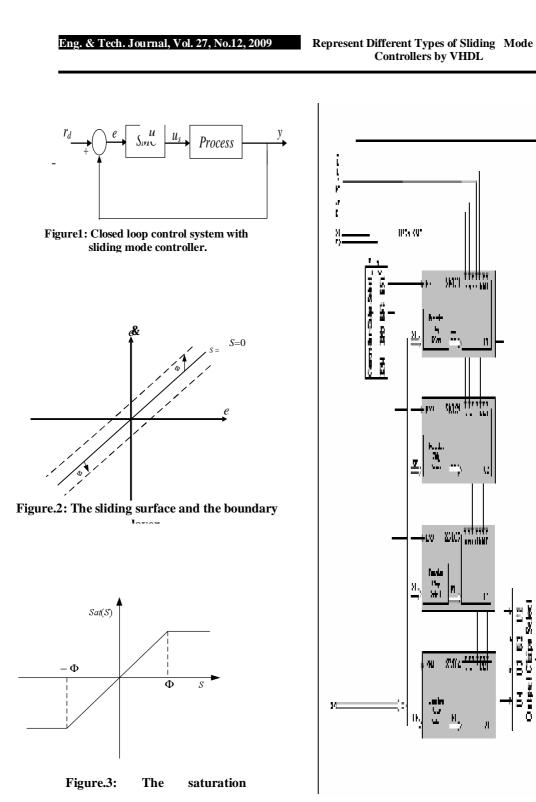


Figure. 4: The proposed FPGA design for SMCs.

Represent Different Types of Sliding Mode Controllers by VHDL

Name	Val				h - 140 T
			Stimulator	1 · 20 · 1 · 40 · 1 · 60 · 1 · 80 · 1 · 100 132.7 ns	1 . 140
+ - s	0		<= 00		
🕀 🗢 EN	J1			(1	
🛨 🖻 SF	• 0		<= 00	0	
🛨 🗢 FI	1			(1	
P- c	2.0	000	<= 2.0	(2.0000	
⊳k	10.0	000	<= 10.0	(10.000	
D- e	-1.4	1000	<= -1.4	(0.40000 X-2.4000 X-1.4	000
⊳- ce	2.8	000	<= 2.8	(0.20000 X2.80	000
-• u	0.0	0000		(10.000 X-10.000 X0.00	0000
					+ 0 + 4
🗐 sr	mc1.vhd	🚵 waveforr	n e		
🗐 sr				March 04, 2008	▶ 4 <u>©</u> H

Figure. 5: General sliding mode controller with sliding function of Eq.(1)

ame	Volum	Stanulator				1 198 1 - 190	
Þ-5.	1	<= 01	(1		112.7 16		
- EN	2	c= 0010	¢2				-
D- 58	0	c= 00	(C				-
- Pt	1		(1				
D⊢ p	1.0000	<= 1.0	(1.0000				
r⊳ k	10.000	c= 10.0	(10.000				
D-F	0.50000	c= 0.5	(0.50000				_
D- e	0.0032000	c= 0.032	(0.53000)		(-0.40000	X0.032000	
D- ce	0.0019000	<= 0.0019	(0.0029000)		(-0.23000	X0.0019000	_
-0 u	0.10200		(10.000)	0.102	00 (-10.000	X0.67800	
			1			+ - 2	-
waveform	n.e						
			inished. There are no more test y		one ha ete	n late	-
				Longer P.	other first sectors	and and an	_

Figure. 6: SMC with boundary layer with saturation function with sliding Function of Eq.(1) when s< Φ and when s>= Φ

X 🖻 🖻				
Name	Value	Stimulator	1 • 20 • 1 • 40 • 1 • 60	69.4 ns
± ⊳ s	2	<= 10	(2	
🗉 🖻 SF	0	<= 00	0	
🗄 🗢 FI	1		(1	
P- c	1.0000	<= 1.0	(1.0000	
₽- F	0.50000	<= 0.5	(0.50000	
₽ k	6.0000	<= 6.0	(6.0000	
₽- ki	0.30000	<= 0.3	(0.30000	
⊳ e	0.013800	<= 0.7604	(0.010900 X0.013800	0.76040
P- ce	0.0073000	<= 0.0259	(0.0017000 X0.0073000	(0.025900
-• u	2.0532		(1.9512)(2.0532)	(6.0000
				▶ 4 0 ₩
🚵 waveform	i e			

Figure. 7: SMC with PI sliding control law with sliding function of Eq.(1)

Represent Different Types of Sliding Mode Controllers by VHDL

Eile Edit	Search View Desig		Waveform To		⇔ »
1			♀ ™ ∅	4 G G	
X PB		⊇ ↔ 🖓	$\mathbf{Q} \mathbf{Q} \mathbf{Q} \mathbf{Q} \mathbf{Q} \mathbf{Q} \mathbf{Q} \mathbf{Q} $		
Name	Value	Stimulator	1 20	24.9 ns	60 • • • 80 • •
∓ ⊳ s	2		(2		
🛨 🖻 SF	2		(2		
🛨 🗢 FI	2		(2		
P- c	1.0000		(1.0000		
₽- c1	2.0000		(2.0000		
P- f	0.50000		(0.50000		
₽- k	6.0000		(6.0000		
⊳- ki	0.30000		(0.30000		
⊳-e	0.010900		(0.010900	X0.013800	X0.025600
₽- ce	0.0017000		(0.0017000	X0.0073000	X0.0087000
🗢 vin	0.032300		(0.032300	X0.054900	X0.078600
🛨 🖻 ez	(0.0091000,0		\langle	X	X(0.0042000,0.0033)
-0 u	2.7264		(2.7264	X2.8284	X2.9868
			•		+ 9 + 4

Figure. 8: PI sliding mode controller with sliding function of Eq.(2)

<u>File E</u> dit Searc	:h <u>V</u> iew <u>D</u> esign	Simulation W	avetorm <u>T</u> ools <u>H</u> elp	<;> >>	
12 🖛 🖆 🔚	** % 🖷	📃 🔎 📶 🤇	🏹 🖓 😵 🖗	5) d d e e e e e e e e e e	
※ ☜ ☜ 🗠 🖓 💫 ♣ 🍕 🔍 ♣ 🔍 ♣ 🖓 ⊐ा № 🎽					
Name	Value	Stimulator	ı · 20 · ı · 40 44	ns 10 · 1 · 80 · 1 · ns	
🗉 🗢 EN	4		(4		
🕀 🗢 FI	3		(3		
Phile	1.0000	<= 1.0	(1.0000		
Ph f	0.50000	<= 0.5	(0.50000		
Ph k	6.0000	<= 6.0	(6.0000		
P≘ ki	0.30000	<= 0.3	(0.30000		
Phe e	0.013800	<= 0.0176	(0.010900 X0.013800	X0.017600	
🛨 🖻 ez	(0.010200,0			χ(0.019800,0.02760)	
🗢 vin	0.085700		(0.032300 X0.085700	X0.16200	
-• u	2.9940		(2.3184 X2.9940	X3.9552	
			·	40 + 4	
🚵 waveform e					

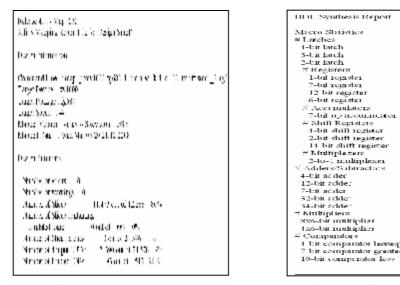
Figure. 9: PI sliding mode controller with sliding function of Eq.(3)

X 🖻 🖻	10 CH A	Q 🕹 🖓 🖓	Q Q Q 🔍 🐄 봬 🗤 AR 📾 💷 🎽
Name	Value	Stimulator	16.2 ns 40 · 1 · 60 · 1 · 80 · ns
± ⊳ s	3	<= 11	(3
🗉 🗢 EN	8		(8
🖅 🖻 SF	0	<= 00	0
🛨 🗢 FI	1		(1
P- c	1.0000	<= 1.0	(1.0000
₽- f	0.50000	<= 0.5	(0.50000
₽- k	10.000	<= 10.0	(10.000
⊳-e	0.022600	<= 0.0305	(0.0226 <mark>00) (0.026700) (0.030500) (0.026700) (0.030500)) (0.030500) (0.030500) (0.030500) (0.030500) (0.0</mark>
P- ce	0.0039000	<= 0.0033	(0.0039000 X0.0037000 X0.0033000
-¤ u	0.50332		(0.50332 X0.57315 X0.63320 ▼

Figure. 10: Boundary SMC with new approximation sign function with sliding function of Ea.(1)

光回日		२ म्म दिशा (Q Q Q Q ()	Su vu Vi	-±10 U.4- >>
Name	Value	Stimulator	1 . 20 . 1 .	4 39.9 ns 80 · ·	- 8,0 - i na
+ - s	3	<= 11	(3		_
🕂 🗢 EN	8		(8		
∓ ⊳ sF	2	<= 10	(2		
🗩 🗢 FI	2		(2		
₽-c	1.0000	<= 1.0	(1.0000		
₽- c1	2.0000	<= 2.0	(2.0000		
₽- F	0.50000	<= 0.5	(0.50000		
⊳ k	10.000	<= 10.0	(10.000		
⊳-e	0.022600	<= 0.0267	(0.022600	0.026700	X0.022600
₽- ce	0.0039000	<= 0.00397	(0.0039000	0.0039700	<u>X0.003900</u>
🛨 🖻 ez	(0.017600,0		(0.017600,0.0138	00,0.010900,0.00	91000,0.400,1
🗢 vin	0.059000		(0.059000	0.11800	<u> </u>
-¤ u	2.2420		(2.2420	3.4783	X2.2420
			•		++0+

Figure. 11: Boundary SMC with new approximation sign function with sliding function of Eq.(2)



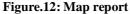


Figure.13: Synthesis report

4 Comparators 4 bit comparator lessequal 7 bit comparator greatecual 10-bit comparator less

HDL Synthesis Report

- 3 ï

: 14 : 1 12 6 : 4 : 2 : 30 : 30 : 22

: 8 : 8 -1 : 1

: 2 : 20

ີ:12 :6 :2

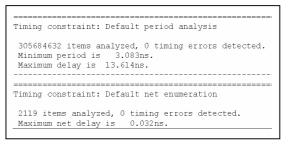


Figure. 14: Timing constraint report

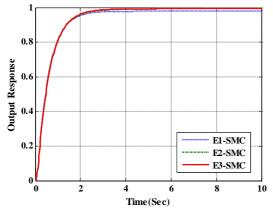


Fig. 15a: The output response of ESMCs for the linear system of example(1) with a unit step input.

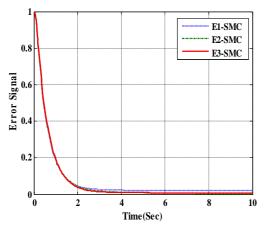


Fig. 15b: Error signal curves for linear system of example(1) with ESMCs.

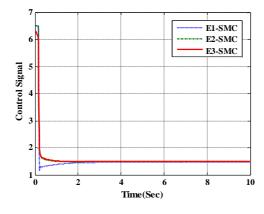


Fig. 15c: Control signal curves for linear system of example(1) with ESMCs.

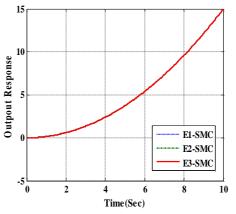


Fig.16a: The output response of ESMCs with linear second order system of example(2) with a parabolic input.

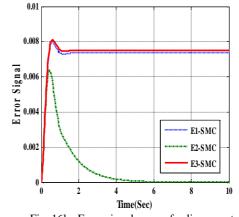


Fig. 16b: Error signal curves for linear system of example(2) with ESMCs.

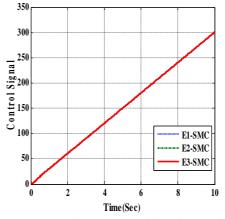


Fig. 16c: Control signal curves for linear system of example(2) with ESMCs.

Represent Different Types of Sliding Mode Controllers by VHDL

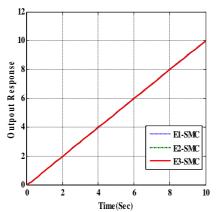
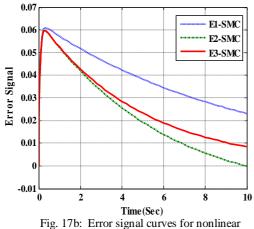
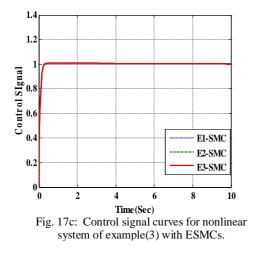


Fig. 17a: The output response of ESMCs with nonlinear system of example(3) with a ramp input.



system of example(3) with ESMCs.



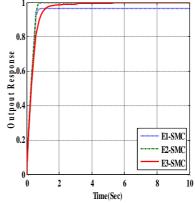
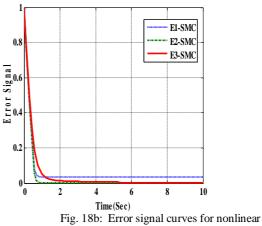
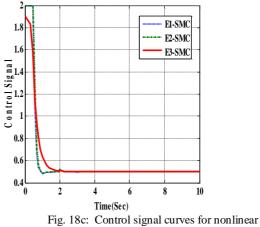


Fig.18a: The output response of ESMCs with nonlinear system of example(4) with a unit step input.



system of example(4) with ESMCs.



system of example(4) with ESMCs.

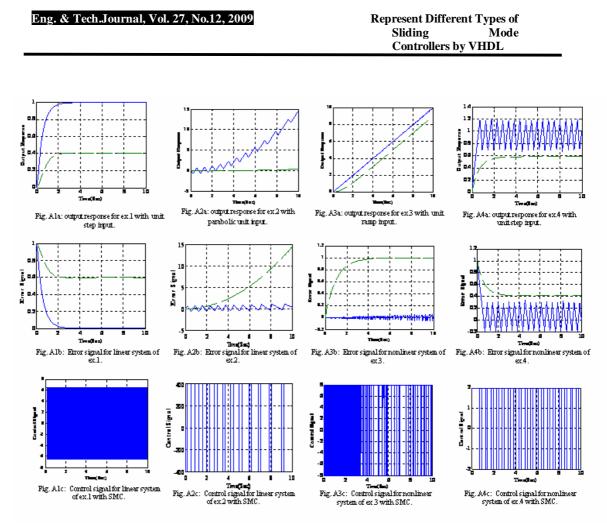
2512

Appendix A

This appendix illustrate the simulation results (output response, error signal, and control signal) of the four examples that are given in section VI when the control system uses the conventional SMC(u=Ksgn(S)) with sliding function of Eq.(1) for examples 1,2,4 and with sliding function of Eq.(2) for example 3. The inputs and the control parameters with this controller for each example are given in Table (A.1), the values of *K* parameters are same the values of *K* in the ESMCs approaches except in example 2 and 4. Also this appendix illustrate the response of the tested example (with unity feedback) without controller.

Table (A.1): input and parameters for the simulation examp								
Example	Type of input	Κ	1	I_i				
No.								
Ex.1	Step input	6.5	2					
Ex.2	Parabolic input	-400	-6					
Ex.3	Ramp input	8		0.1				
Ex.4	Step input	-2	-8					

The results for the simulation examples are shown in the following figures, where the *dished line* '---' refer to response of these examples without controller, while the *sold line* '___' refer to response of these examples with the conventional SMC.



Appendix B

This appendix illustrate the simulation results (output response, error signal, and control signal) of two additional examples, the first one is linear unstable system with $G(s) = \frac{1}{(s^2 - 5)}$ which has two root lies at the right half plane, the second one is linear time varying model $\Re(t) = a(t)y(t) + b(t)u(t)$, where a(t)=0.001t and b(t)=0.15t, t is varying from zero to 10Sec. The sliding functions, types of controllers and the control parameters that are used for controlling these examples are given in Table(B.1) and Table(B.2). This appendix also illustrates the response of these simulated examples without controller (with unity feedback).

Table (B.1): types of controllers and control parameters for the linear unstable example

SMC type	K	Φ	l_i	K _I	1	
E2-SMC	35	0.5			3	

Table (B.2): types of controllers and control
parameters for the linear time varying example.

SMC type	K	Φ	1 _i	K _I	1
E1-SMC	4	0.5	.00001		2

Represent Different Types of Sliding Mode Controllers by VHDL

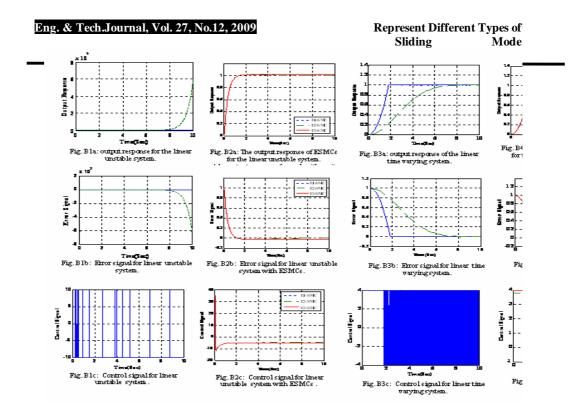
2

2

2

E2-SMC	35	0.5		0.3	3	E2-SMC	4	0.5	.00001	.0001
E3-SMC	35	0.5	.005		3	E3-SMC	4	0.5	.0002	
Conventional SMC	10				3	Conventional SMC	4		.00001	

If reference is unit step signal, then the results for the simulation examples are shown in the following figures. As in appendix A, in the figures without legend, the *dished line* '---' refer to response of these examples without controller, while the *sold line* '___' refer to response of these



examples with the conventional SMC. We observed from Fig.B2 and Fig.B4, that all the ESMCs approaches track the desired input signal, with zero or a small steady state error.