


## **Implementing of Forward Link Channel CDMA2000-1x System by Using Simulink HDL Coder**

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### **ABSTRACT**

This work is a proposed simulation for forward link channel of CDMA2000 -1x system by using QPSK, 8QAM and 16QAM, and converting the proposed system to VHDL language by using Simulink HDL Coder for implementing in FPGA board.

The results of simulation for forward link channel of CDMA2000 system shows improvement when using three levels of codes (LPNC, Walsh code and complex coding) in the present of AWGN for QPSK modulation the system performance is improved from (1.8 to 1.9) in dB for BER (Bit Error Rate)  $10^{-4}$  to  $10^{-5}$  and for 8QAM the system performance is improved at (2.9) in dB for BER  $10^{-4}$  to  $10^{-5}$  and for 16QAM the system performance is improved from (1 to 1.2) in dB for BER  $10^{-4}$  to  $10^{-5}$ . The results of simulation in the present of AWGN and Rayleigh fading channel are improvement within (0.5) in dB for the different Doppler Frequencies (5 - 230Hz).

The Simulink HDL Coder has been used for converting the MATLAB-Simulink models to VHDL language. The verification of the generated VHDL code has been done using Altera-ModelSim program, while the synthesis reports and board programming files have been obtained using the Quartus II program. System implementation has been done using FPGA technology with Altera Cyclone II boards. The implementation of the forward link channel by using Simulink HDL coder shows feasibility and flexibility in solving the problem of complex multiplication of complex spreading code also the practical results were closed to that obtained from ModelSim program.

**Keywords:** CDMA, FPGA, LPNC, VHDL

## تنفيذ لقناة الوصلة الامامية لنظام التقسيم الشفري لتعدد الوصلية (CDMA2000-1x) باستخدام مشفر لغة الكيان المادي الكتلي (Simulink HDL Coder)

### الخلاصة

أقترح هذا العمل محاكاة لقناة الوصلة الامامية لنظام التقسيم الشفري لتعدد الوصلية (CDMA-2000) باستخدام تقنية التضمين (QPSK, 8QAM and 16QAM) وتحويل النظام القترح الى لغة VHDL باستخدام مشفر لغة الكيان المادي الكتلي (Simulink HDL coder) لتطبيقه على لوحة مصفوفة البوابات المنطقية الواسعة (FPGA). نتائج محاكاة قناة الوصلة الامامية لنظام التقسيم الشفري لتعدد الوصلية (CDMA-2000) عند استعمال ثلاث انواع من الشفرات (الشفرة الطويلة للضوضاء المزيفة (LPNC)، شفرة Walsh و التشفير المركب) في حضور الضوضاء حُسن اداء النظام لتضمين (QPSK) من (1.8 الى 1.9) (dB) ضمن نسبة خطأ  $10^{-4}$  الى  $10^{-5}$  و حُسن اداء النظام لتضمين (8QAM) عند (2.9) (dB) ضمن نسبة خطأ  $10^{-4}$  الى  $10^{-5}$  و حُسن اداء النظام لتضمين (16QAM) من (1 الى 1.2) (dB) ضمن نسبة خطأ  $10^{-4}$  الى  $10^{-5}$ . نتائج المحاكاة بحضور الضوضاء والخفوت تحسنت بمقدار 0.5 (dB) لمختلف ترددات دوبلر (5 - 230) Hz.

تم استخدام مشفر لغة الكيان المادي الكتلي (Simulink HDL Coder) لغرض تحويل (MATLAB-Simulink models) الى لغة (VHDL). تمت عملية التحقق من الكود باستخدام برنامج (ModelSim-Altera) اما نتائج البناء وعملية تحميل البيانات وملفات البرمجة تمت باستخدام برنامج (Quartus II). تم بناء النظام باستخدام تقنية مصفوفة البوابات المنطقية الواسعة (FPGA) مع Altera Cyclone II board. بناء قناة الوصلة الامامية بواسطة استعمال مشفر لغة الكيان المادي الكتلي (Simulink HDL coder) الذي بين الملائمة والمرونة من خلال حل مشكلة الضرب المعقد لشفرة الانتشار المعقدة وكذلك كانت النتائج العملية مقارنة لما تم الحصول عليه من برنامج (ModelSim).

### INTRODUCTION

Direct sequence CDMA (DS-CDMA) is the most popular of CDMA techniques. The DS-CDMA transmitter multiplies each user's signal by a separate code waveform. The signals of all users overlap and interfere with each other in a DS-CDMA system; the receiver recovers the signals by correlating the combined signal with the code of the desired user [1].

The third generation CDMA came through a detailed proposal process from vendor's interested in the evolution of IS-95B. The IS-95B standardization adopted a framework that combined the different vendor's proposals and later became known as CDMA2000. CDMA2000-1x is a family of 3G mobile technology standards, which use CDMA channel access, to send voice, data, and signaling data between mobile phones and cell sites. The set of standards includes: CDMA2000-1X, CDMA2000-EV-DO, CDMA2000-EV-DV, and CDMA2000-3x [2].

However, implementing of CDMA2000-1x system with flexibility remains the main problem to born the practical system. MathWorks introduced Simulink HDL Coder, which automatically generates synthesizable Hardware Description Language (HDL) code from models created in the company's widely-used Simulink and Stateflow software. The product produces target-independent Verilog and VHDL code and test benches for implementation and verification by using FPGA. Simulink HDL Coder accelerates the design, implementation, and verification of hardware, by providing a path directly from system models to programing FPGA. Simulink HDL Coder also generates Verilog and VHDL test benches that enable reusing system simulation data for verification of the implemented design [3].

**PROPOSED SYSTEM DESIGN**

The proposed design procedure for FFCH-DS-CDMA2000-1x is shown in figure (1) and table (1) shows the proposed design parameters of the system. The main parts of the proposed system are in the following sections.

**Long PN Code Design**

Pseudo-Noise (PN) code sequence acts as a noiselike (but deterministic) carrier used for bandwidth spreading of the signal energy. The selection of a good code is important, because type and length of the code sets bounds on the system capability. The PN code sequence is a Pseudo-Noise or Pseudo-Random sequence of 1's and 0's, but not a real random sequence (because periodic). Random signals cannot be predicted. Maximal length sequences (which are also called m-sequences, pseudo random sequences or pseudo noise sequences) are certain binary sequences of length [4].

$$N = 2^n - 1 \tag{1}$$

Where n = number of shift register. The long code in CDMA2000 consists of 42 shift register with mask  $(2^{42} - 1)$ , the recursion for the long code spreading is generated by the characteristic polynomial p(x) [4,5]:

$$P(x) = x^{42} + x^{35} + x^{33} + x^{31} + x^{27} + x^{26} + x^{25} + x^{22} + x^{21} + x^{19} + x^{18} + x^{17} + x^{16} + x^{10} + x^7 + x^6 + x^5 + x^3 + x^2 + x + 1 \tag{2}$$

**Walsh Code Design**

Walsh codes are the most common orthogonal codes used in CDMA applications. The Walsh codes are generated in a set of codes with length  $(N = 2^n)$ . The generating algorithm is given by [5]:

$$W_N = 0, W_{2N} = \begin{pmatrix} W_N & W_N \\ W_N & \overline{W_N} \end{pmatrix} \tag{3}$$

The rows (or columns) of the matrix  $W_N$  are the Walsh codes. In each case the first row (row 0) of the matrix consists entirely of (1s) and each of the other rows

contains  $N/2$  of (0s) and  $N/2$  of (1s). The distance (number of different elements) between any pair of rows is exactly  $N/2$ . Each sequence of  $n$  bits identifies one row of the matrix (there are  $N = 2^n$  possible rows). All rows are mutually orthogonal [5].

**Short Code Design (PN<sub>I</sub> and PN<sub>Q</sub>)**

The short code is generated by a 15-stage shift-register circuit ( $2^{15} - 1$ ) chips arranged to produce the polynomials given by equations (5) and (6). Each of the circuits generates 32767 chip long sequences ( $2^N - 1$ ) composed of 16384 ‘1s’ and 16383 ‘0s’. The transmission rate of these sequences is 1.2288 Mcps, the sequence has a repetition rate of 37.5 times per second (1228800 cps/32768cps = 37.5 times/s) [4,5].

$$PI(x) = x^{15} + x^{13} + x^9 + x^8 + x^7 + x^5 + 1 \quad (4)$$

$$PQ(x) = x^{15} + x^{12} + x^{10} + x^6 + x^5 + x^4 + x^3 + 1 \quad (5)$$

**Digital Arm Filter Design**

Raised Cosine Filter is used in order to remove the high frequency components from the output of multiplier. The two digital arm filters in transmitter must have the same design to avoid jitter and the order is not too high because that means delay. Table (2) shows the parameters selected for the filter. **This filter will be FIR filter because it has linear frequency response [6]. The transfer function is given by:**

$$H(z) = \sum_{n=0}^{N-1} h(n) Z^{-n} \quad (6)$$

The frequency response is given by:

$$H(e^{jw}) = \sum_{n=0}^{N-1} h(n)e^{-jwn} \quad (7)$$

where  $h(n)$  is the impulse response of the FIR filter, the hamming window is given by [6]:

$$\omega(n) = 0.54 + 0.46\cos(2\pi n/M) \quad (0 < n \leq M) \quad (8)$$

$$h_D(n) = 2f_c \sin(2\pi f_c n) / 2\pi f_c n \quad n \neq 0 \quad (9)$$

$$h_D(n) = 2f_c \quad n = 0$$

$$h(n) = h_D(n) \times \omega(n) \quad (10)$$

Where  $n = 0, 1, 2, \dots, M - 1$ ,  $\omega(n)$  is the window function,  $h_D(n)$  is the desired impulse response of the filter,  $f_c$  is chosen proportional to sampling rate,  $M$  is the filter order.

**Modulation Technique**

Multilevel Quadrature Amplitude Modulation (M-QAM) is used in CDMA2000-1x to obtain higher spectral efficiency, which potentially results in higher throughput of packetized data. The QAM signal points lie in rectangle or square instead of circle as in QPSK. In QAM modulator both the amplitude and the phase of the bandpass signal will be changed, so it's PSK and ASK occur at the same time. The M- QAM signal is given by [7]:

$$s(t) = A(t)[\cos(\phi(t)) \cos(2\pi f_c t) - \sin(\phi(t)) \sin(2\pi f_c t)] \quad (11)$$

Where:  $A(t)[\cos(\phi(t))]$  represent the amplitude of I-channel,  $A(t)[\sin(\phi(t))]$  represent the amplitude of Q-channel and  $f_c$  is the carrier frequency and  $t$  is the time.

Multilevel Quadrature Amplitude Modulation (M-QAM) extends QAM by making the size of the transmitted constellation variable. The variable constellation size means that the number of bits per symbol is also variable. The number of bits that can be sent per symbol,  $N$ , in a square constellation is related to  $M$  as  $N = \log_2 M$  (where  $M =$  number of levels) (also number of bits increases) the information can be sent also increases as long as the symbol rate remains constant. This leads to the possibility of variable bit rate operation in a constant bandwidth [7].

**Decision Circuits**

The probability of error depends on the characteristic of decision circuit. There are two types of decision circuit hard and soft. In Hard Decision Decoding (HDD) each coded bit is demodulated as 0 or 1, the demodulator detects each coded bit (symbol) individually. The received symbol is decoded as 1 if it is closer to  $\sqrt{E/2}$  ( $E$  is energy per bit) and as 0 if it is closer to  $-\sqrt{E/2}$ . Soft decision is the second method of implementation in which the detector outputs a multilevel voltage and the channel decoder bases its output on these inputs. Soft decision provides about 2-3db coding gain over hard decision but increases the system cost because it requires an error correction code which means more complication and more cost [8].

In this work hard decision is used for QPSK because hard decision has the ability to distinguish between small amplitudes bits, and soft decision is used for M-QAM modulation to distinguish between large amplitude bits. Figures (2) and (3) show the soft and hard decisions block diagram respectively.

**SIMULATION RESULTS**

In this work the simulation of the proposed CDMA2000 system in the presence of Additive White Gaussian Noise (AWGN) and Rayleigh fading channel.

Different modulation types are used (QPSK, 8QAM and 16QAM) in the proposed system. A MATLAB (2009) is used in the simulation and performance evaluation of the proposed system.

Simulation Results for the Proposed System without Codes includes the performance evaluations of the different modulation / demodulation schemes which are used in the proposed system (QPSK, 8QAM and 16QAM) with AWGN and Rayleigh. In this stage of the simulation and the variation of the Bit Error Rate (BER) are performed according to the variation ratio for energy of data bit to the power spectrum density ( $E_b/N_o$ ). Figure (4) shows the performance of modulation over AWGN without codes and figures (5, 6 and 7) show the performance of modulation with (QPSK, 8QAM and 16QAM) without codes over AWGN and Rayleigh fading channel with different values of Doppler frequencies.

The performance of CDMA2000 using QPSK modulation system will be evaluated by plotting the BER versus the ( $E_b/N_o$ ) in the presence of AWGN and Rayleigh fading for different values of Doppler frequencies. Figure (8) shows the effect of AWGN over QPSK modulation and figure (9) shows the effect of AWGN and Rayleigh fading channel on the system.

The performance of CDMA2000 using 8-QAM modulation system will be evaluated by plotting the BER versus the ( $E_b/N_o$ ) in the presence of AWGN and Rayleigh fading for different values of Doppler frequencies. Figure (10) shows the effect of AWGN over 8-QAM modulation and figure (11) shows the effect of AWGN and Rayleigh fading channel on the system.

The performance of CDMA2000 using 16-QAM modulation system will be evaluated by plotting the BER versus the ( $E_b/N_o$ ) in the presence of AWGN and Rayleigh fading for different values of Doppler frequencies. Figure (12) shows the effect of AWGN over 16-QAM modulation and figure (13) shows the effect of AWGN and Rayleigh fading channel on the system.

### **IMPLEMENTING OF FFCH-DS-CDMA2000-1X BY USING SIMULINK HDL CODER**

The proposed system has been designed and implemented based on Simulink HDL coder using FPGA. MATLAB-Simulink is used as an attractive simulation tool which provides the designer with many facilities such as fast design, and procedure test. Also, it gives the designer a clear imagination of the system parameters required to complete the design. MATLAB-Simulink of MATLAB (2009) is used in this work. Simulink HDL coder is a tool, which comes with MATLAB-Simulink software package and can be used to generate Hardware Description Language (HDL) code based on Simulink models and Stateflow finite-state machines. In this work, the design is first implemented in MATLAB-Simulink environment. It is then converted to VHDL level using the signal compiler block of the Altera-DE2-70 Board. The design is synthesized and fitted with Quartus II software, and downloaded to Altera-DE2-70 development board. Figure (14) shows the Photograph of the FPGA board and figure (15) shows the Altera-DE2-70 development board. The implementing of the proposed system according to the following steps:

### **Setting Parameters**

To start the implementation of the proposed system, the parameters of the proposed system should first be set, system parameters setting include specification of the different types of codes, modulation/demodulation and other related system operations that the SDR could handle.

### **Verifying Design Functionality**

Some MATLAB-Simulink blocks, especially those that contain complex functions could not be converted to VHDL codes. To solve this problem, these blocks are redesigned using their basic components such that they could be converted to VHDL codes.

The modulations and demodulations are designed using embedded MATLAB functions (m-files), while other blocks are designed by MATLAB-Simulink blocks supported by Simulink HDL coder.

### **Generating Vhdl Codes For Matlab-Simulink Using Simulink Hdl Coder**

Simulink HDL Coder compatibility checker utility can be run to examine MATLAB-Simulink model semantics and blocks for HDL code generation compatibility, then by invoking the coder, using either the command line or the graphical user interface. The coder generates VHDL or Verilog code that implements the design embodied in the model. Usually, a corresponding test bench can also be generated. The test bench with HDL simulation tools can be used to drive the generated HDL code and evaluate its behavior. The coder generates scripts that automate the process of compiling and simulating the code in these tools.

### **Verifying Design Functionality Using (Modelsim Tool)**

The correct functionality of SDR is verified using Altera / Mentor Graphics ModelSim (6.5b) simulation tool. For this purpose, the test bench codes are compiled and simulated using the generated compilation and simulation scripts by the HDL coder.

### **Designing Synthesis using Quartus II**

Designing Synthesis is a process that starts from a high level of logic abstraction (typically Verilog or VHDL) and automatically creates a lower level of logic abstraction using a library of primitives [9].

### **Downloading Bit Stream File to FPGA Boards**

The synthesis process would also produce a bit stream file that can be downloaded in the FPGA board. The bit stream file of the SDR has been successfully downloaded to Altera-Cyclone II FPGA family boards, which is Cyclone II DE2-70. The test operation of the physical functionality of the SDR has been done by simply interfacing a function generator to apply input data and oscilloscope to monitor the recovered data.

Figure (16) shows the input and output waveforms of the proposed CDMA2000 system with QPSK modulation by using ModelSim program and figure (17) shows these input and output data from an oscilloscope.

Figure (18) shows the input and output waveforms of the proposed

CDMA2000 system with 8-QAM by using ModelSim program and figure (19) shows these input and output data from an oscilloscope.

Figure (20) shows the input and output waveforms of the proposed CDMA2000 system with 16-QAM by using ModelSim program and figure (21) shows these input and output data from an oscilloscope.

### DISCUSSIONS OF RESULTS

The performance of the proposed system in the presence of AWGN and Rayleigh fading channel shows improvements compared with the system without long-PN code, Walsh code and complex system as follows:

✓ For simulation

- 1) For FFCh-DS-CDMA2000-1x by using QPSK modulation:
  - For BER  $10^{-3}$  with AWGN, the system performance is improved by (2) dB.
  - For BER  $10^{-4}$  with AWGN, the system performance is improved by (1.8) dB.
  - For BER  $10^{-5}$  with AWGN, the system performance is improved by (1.9) dB.
  - For BER with DF= (5, 45, 90,160 and 230) Hz the system performance is improved by (0.5) dB.
- 2) For FFCh-DS-CDMA2000-1x by using 8QAM:
  - For BER  $10^{-3}$  with AWGN, the system performance is improved by (3.1) dB.
  - For BER  $10^{-4}$  with AWGN, the system performance is improved by (2.9) dB.
  - For BER  $10^{-5}$  with AWGN, the system performance is improved by (2.9) dB.
  - For BER with DF = (5, 45, 90,160 and 230) Hz the system performance is improved by (0.5) dB.
- 3) For FFCh-DS-CDMA2000-1x by using 16QAM:
  - For BER  $10^{-3}$  with AWGN, the system performance is improved by (0.8) dB.
  - For BER  $10^{-4}$  with AWGN, the system performance is improved by (1.2) dB.
  - For BER  $10^{-5}$  with AWGN, the system performance is improved by (1) dB.
  - For BER with DF = (5, 45, 90,160 and 230) Hz the system performance is improved by (0.5) dB.

✓ For implementation



- 1) The experimental results obtained from the implanted system using HDL coder show the flexibility of implementing the forward channel CDMA2000 system.
- 2) The problem of implementing complex multiplication was solved during this work by converting the complex multiplication to the ordinary multiplication by using m-file. This problem is considered the main difficulty in the published literature.

### **CONCLUSIONS**

The following points represent the main conclusions obtained from this work:

- 1) The simulation results of FFCh-SC-DS-CDMA2000-1x system show improvements when using three levels of codes (LPNC, Walsh code and complex coding) within (0.5-2.9)  $E_b/N_0$  in (dB) in the presence of AWGN and Rayleigh fading channel.
- 2) The implementation of the forward link channel using Simulink HDL coder shows feasibility and flexibility of solving the problem of complex multiplication of complex spreading code also the practical results were close to that obtained from ModelSim program.
- 3) Simulink HDL coder is very helpful for system engineers since the coder automates the hardware implementation process. Simulink HDL coder does not support all MATLAB-Simulink blocks, so to generate VHDL codes for such blocks they must be redesigned according to their basic design blocks supported by Simulink HDL coder.

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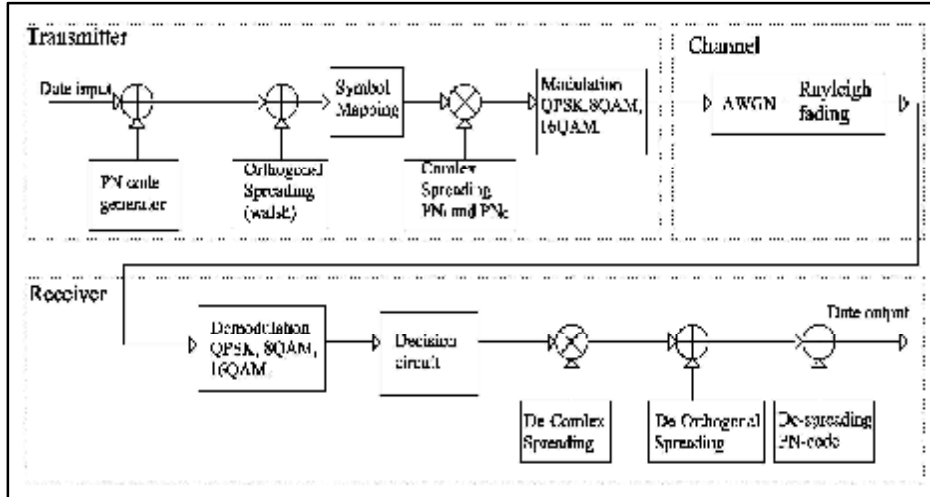


Figure (1): Block diagram of the proposed system.

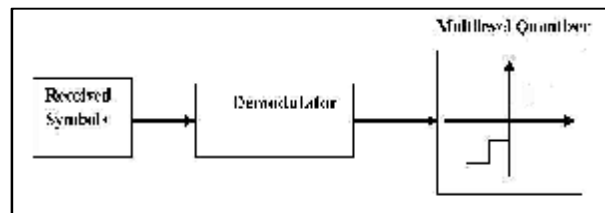


Figure (2): Soft decision decoding.

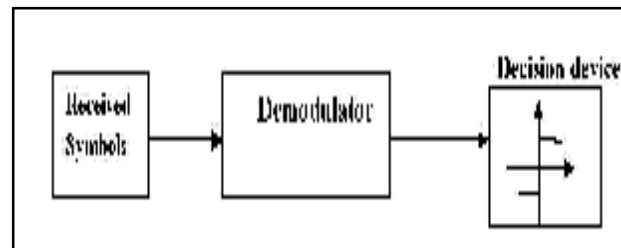


Figure (3): Hard decision decoding.

**Table (1) Design parameters goals**

Parameter	Selected types or values	Comment
Modulation type	QPSK, 8QAM, 16QAM	
Intermediate Frequency (IF)	10MHz	Moderate frequency can be used to implement system
Bandwidth	1.25MHz	standard of CDMA2000-1x
Data rate	(9.6-307.2)Kbps	Suitable data rate can be selected for IT
Doppler Frequency (DF)	5Hz - 200Hz	This value is compatible for CDMA2000
Multiplier	PDF-type	PDF is chosen to provide error signal phase and frequency
Type of filter	Raised Cosine Filter	Suitable filter for CDMA
Decision circuit	Soft and Hard decisions	
Long PN code	$2^{15} - 1$	1.2288Mbps
Walsh code	256	1.2288Mbps
PN <sub>c</sub> and PN <sub>d</sub>	$2^{15} - 1$	1.2288Mbps

**Table (2) Characteristics of the filter**

Filter character	FIR Because it is a linear phase response, and simple in the design
Bandwidth (BW)	1.25MHz
Filter window type	Hanning window is used because of its simplicity and for its accuracy
Filter order	15

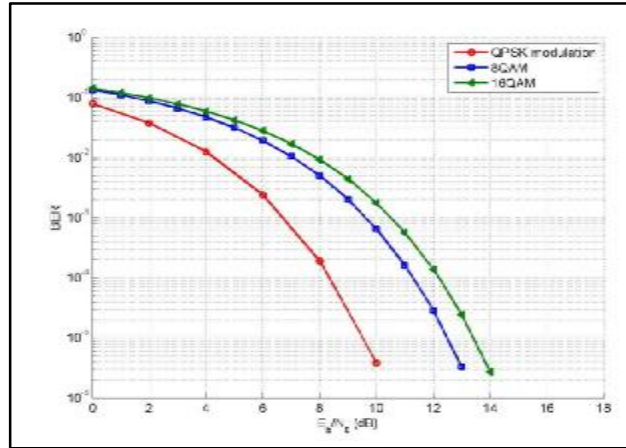


Figure (4): Performance of different modulation schemes over AWGN

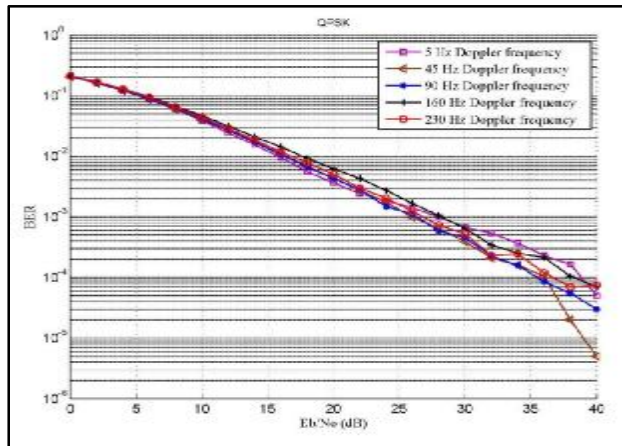


Figure (5): Performance of QPSK over AWGN and Rayleigh fading.

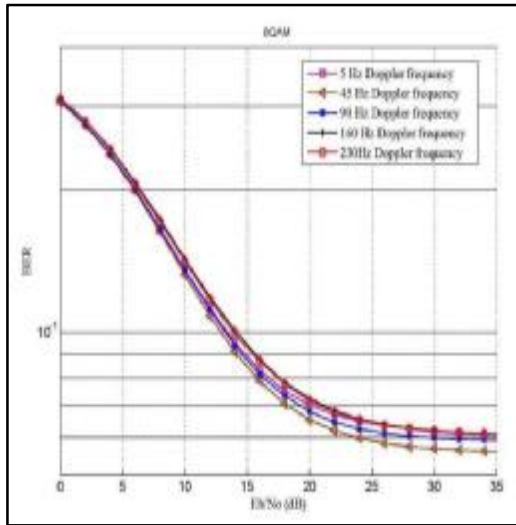


Figure (6): Performance of 8QAM over AWGN and Rayleigh fading.

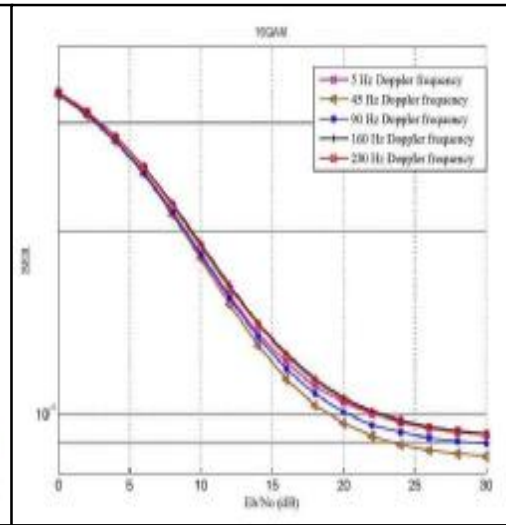


Figure (7): Performance of 16QAM over AWGN and Rayleigh fading.

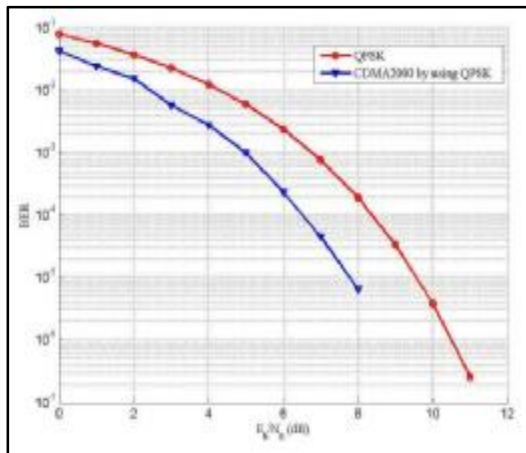


Figure (8): Simulation results of CDMA2000 by using QPSK modulation over AWGN.

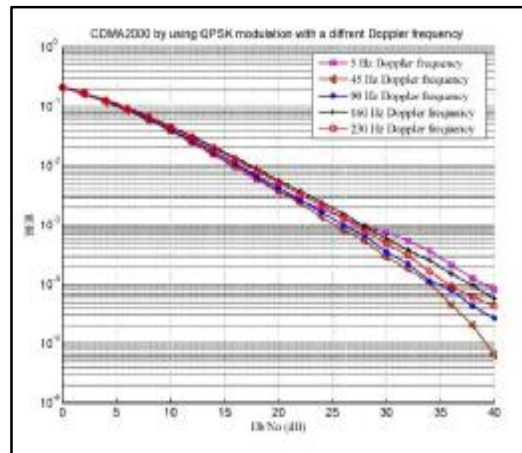


Figure (9): Simulation results of CDMA2000 by using QPSK over AWGN and Rayleigh fading.

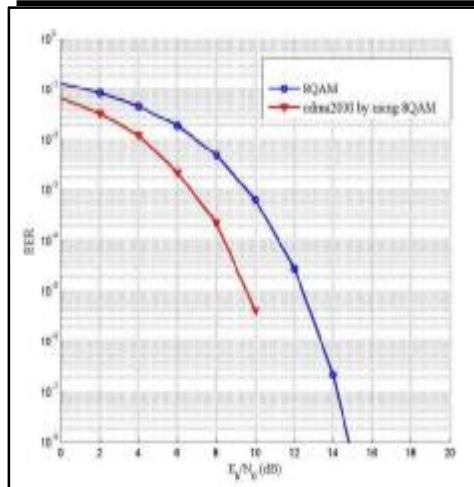


Figure (10): Simulation results of CDMA2000 by using 8QAM over AWGN and Rayleigh.

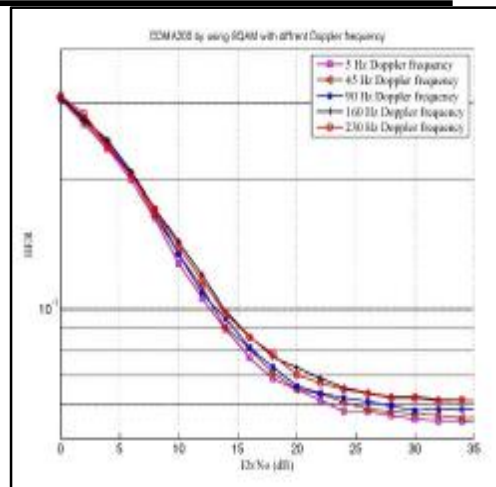


Figure (11): Simulation results of CDMA2000 by using 8QAM over AWGN.

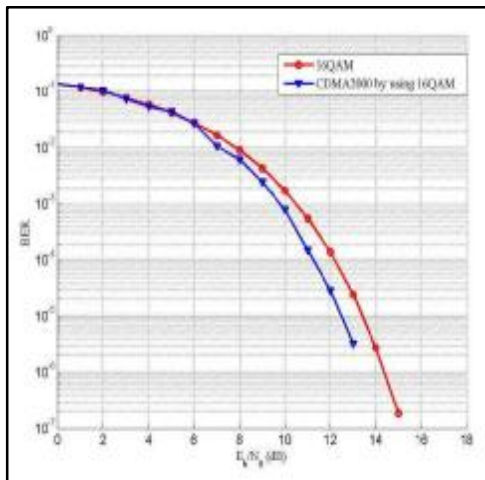


Figure (12): Simulation results of CDMA2000 by using 16QAM over AWGN.

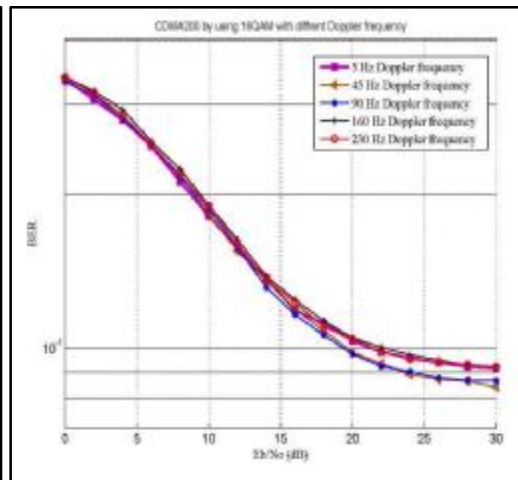


Figure (13): Simulation results of CDMA2000 by using 16QAM over AWGN and Rayleigh.

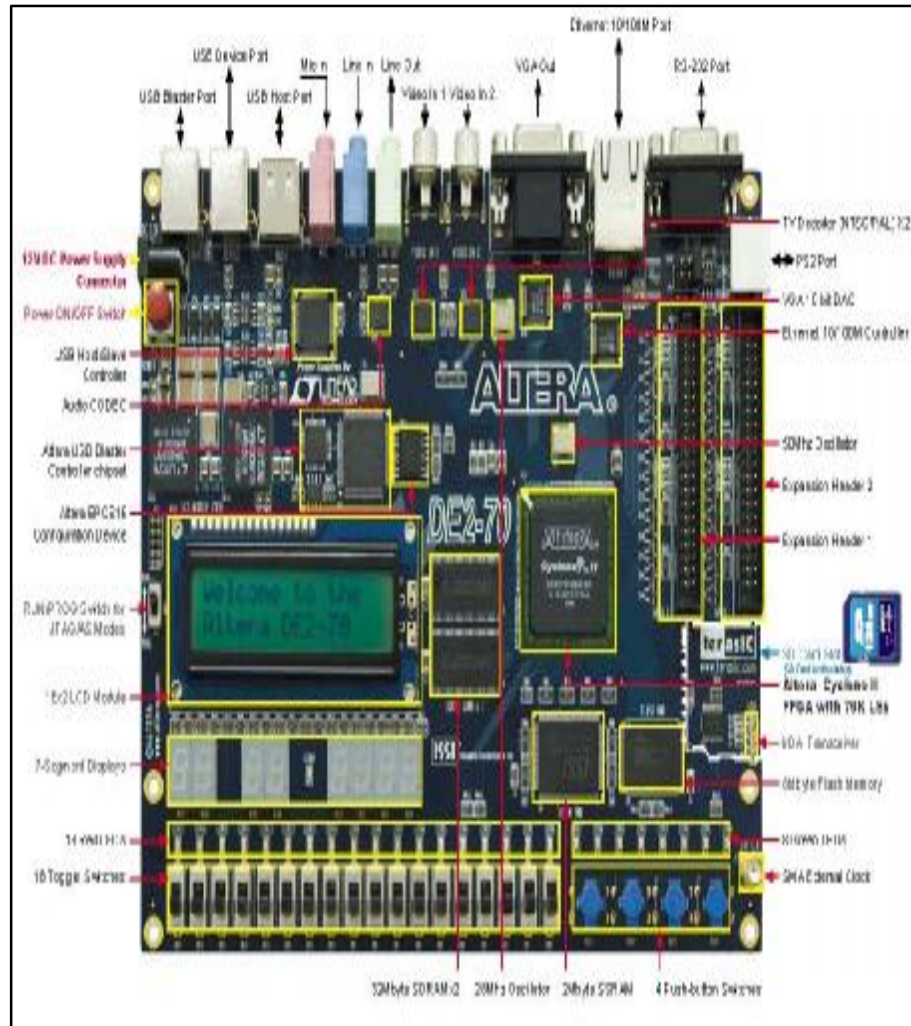


Figure (14): Photograph of the FPGA board.

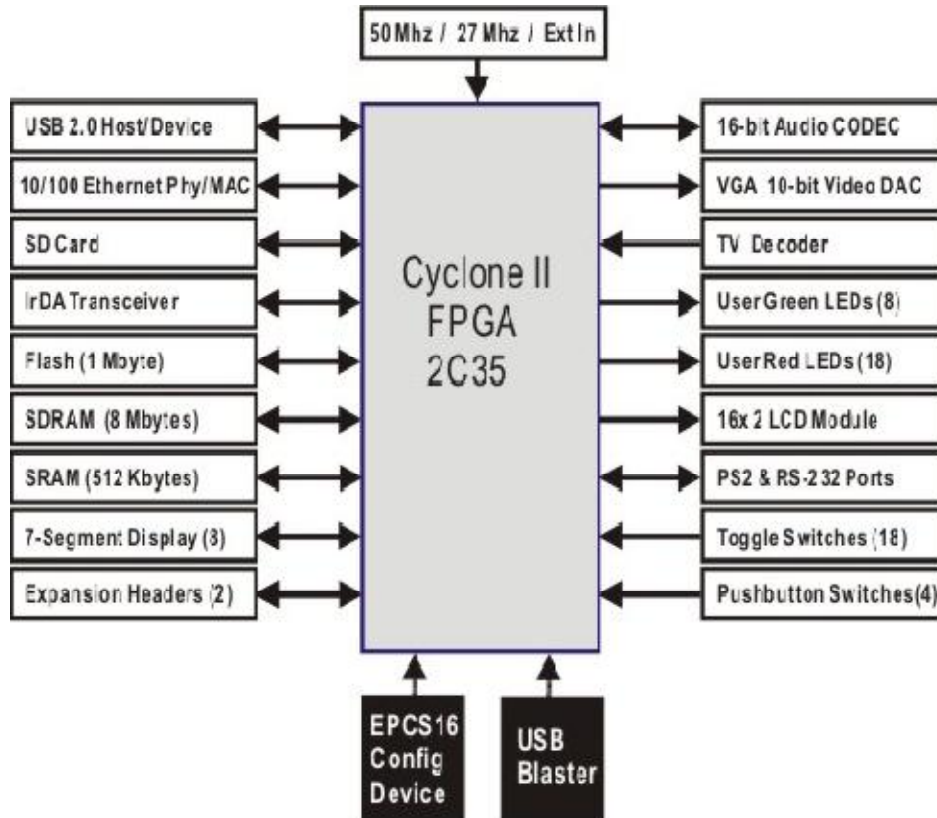


Figure (15): Functional block diagram of the Cyclone II



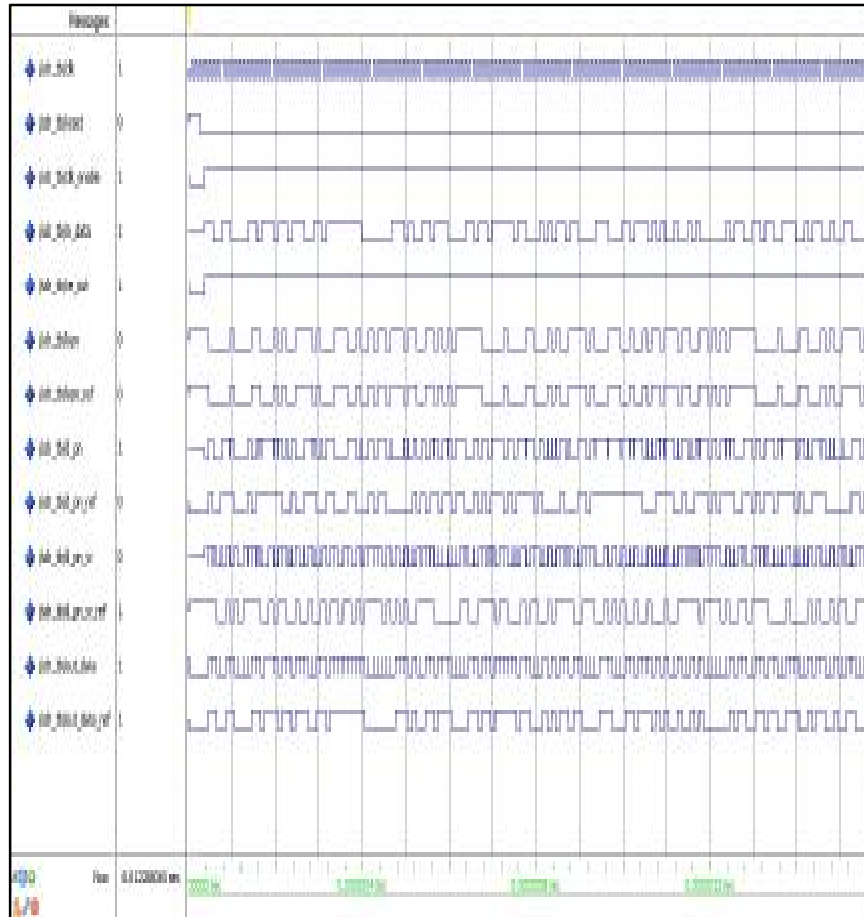


Figure (16): Input and output waveforms of the CDMA2000 system with QPSK modulation in ModelSim program.



Figure (17): Input and output signal from an oscilloscope with 8QAM.

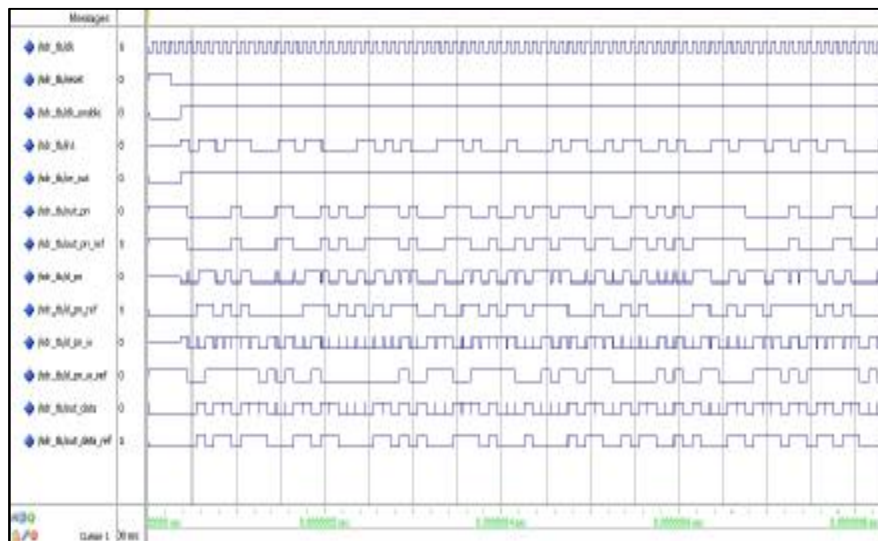


Figure (18): Input and output waveforms of the CDMA2000 system with 8-QAM in ModelSim program



Figure (19): Input and output signal from an oscilloscope with 16-QAM.

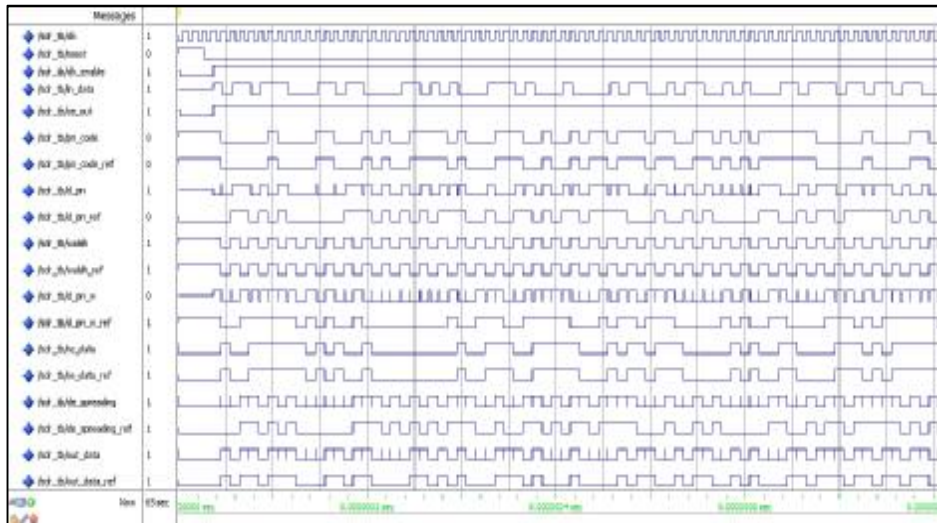
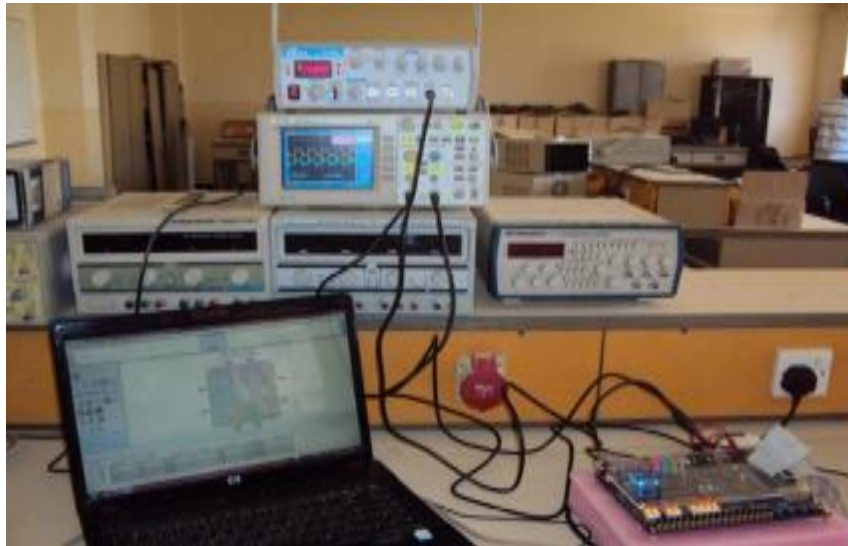


Figure (20): Input and output waveforms of the CDMA2000 system with

16-QAM in ModelSim program



**Figure (21):** Input and output signal from an oscilloscope with 16-QAM.